KODAK

SD Express microSD Card Specification

Version 1.0

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REVISION HISTORY

Revision	History	Draft Date	Remark
V1.0	First release.	2024/11/09	Henry Sun

PRODUCT OVERVIEW

- **Flash Type**
  - KIC BICS5 512Gb
- **Bus Speed Mode**
  - PCIe/NVMe Gen3 x1
  - UHS-I
- **Power Consumption** [Note]
- **UHS-I Mode**
  - Power Up Current ≤ 250uA
  - Standby Current ≤ 1000uA
  - Read Current ≤ 400mA
  - Write Current ≤ 400mA
- **SD Express Mode**
  - Read Current ≤ 400mA
  - Write Current ≤400mA
- **CPRM Optional (Content Protection for Recordable Media)**
- **Advanced Flash Management**
  - Static and Dynamic Wear Leveling
  - Bad Block Management
- **Write Protect with mechanical switch**
- **Supply Voltage**
  - VDD1: 2.7 ~ 3.6V
  - VDD2: 1.7 ~ 1.95 V
- **Temperature Range**
  - Operation: -25°C ~ 85°C (Tc 95C)
  - Storage: -40°C ~ 85°C
- **RoHS compliant**
- **EMI compliant**
- **ESD compliant**

NOTE: Please see Chapter 6.1 Power Consumption for details.

PERFORMANCE

Capacity	PCIe	UHS Speed Grade	VSC	APP Class	Controller	Flash			Performance CrystalDiskMark PCIe[1] (Burst mode)		Performance CrystalDiskMark PCIe[1] (Sustained mode)	
						Density	Process	Bit-per-cell	Read (MB/s)	Write (MB/s)	Read (MB/s)	Write (MB/s)
128GB	Gen3x1	UHS104-U3	V30	A1	5017	512Gbx2	BICS5	TLC	810	500	650	60
256GB	Gen3x1	UHS104-U3	V30	A1	5017	512Gbx4	BICS5	TLC	810	700	650	60

1. The PCIe performance was measured by direct connecting mother board reader
2. The Burst mode size is the 1/8 capacity.

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1. INTRODUCTION

1.1. General Description

The microSD Express card is fully compliant with the standards released by the SD Card Association. The Command List supports the latest SDA Physical Layer Specification definitions. Card capacities of the nonsecure area and secure area (if needed) support [Part 3 Security Specification Ver7.0] Specifications.

The microSD Express card comes with a 17-pin interface, designed to operate at PCIe Interface with a maximum throughput (logical/ideal performance) to 985MB/s (Gen3x1Lane). It can alternate communication protocol between the SD Express mode, SD mode and SPI mode. Backward compatible with UHS-I hosts. It performs data error detection and correction with reasonable power consumption and supports the latest process NAND Flash.

microSD Express card is the first memory card that implements PCIe/NVMe interface and protocol. It is the most slim SSD like storage device with more than 985MB/s speed and. It is designed for those applications that need extreme high performance (ex: burst mode photo shooting, 8K 10K video recording, AR/VR…etc.).We can expect more and more hosts and card readers are supporting SD Express protocol and let removable storage device with high speed transmission securely be highly possible.

1.2. Flash Management

1.2.1. Error Correction Code

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, SD card applies ECC Algorithm, which can detect and correct errors during Read processes, ensuring data is read correctly, as well as protecting data from corruption.

1.2.2. Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some area gets updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

KODAK provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND Flash is greatly improved.

1.2.3. Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. KODAK implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

2. PRODUCT SPECIFICATIONS

- **Capacity:** 128GB/256GB
- **MTBF:** ≧ 3 million hours
- **Bus Speed Mode – using PCIe Differential Interface Lines**
  - PCIe with Gen 3 x 1 Lan – Up to 985MB/s
  - Gen3 x1 bus, two differential I/O(1 RX/ 1TX) of 8Gbps transfer for each direction
    (~1.5% overhead due to 128/120 encoding)
- **Bus Speed Mode – using 4 parallel data lines**
  - **Non-UHS Mode:**
    - Default speed mode: 3.3V signaling, frequency up to 25MHz, up to 12.5 MB/sec
    - High speed mode: 3.3V signaling, frequency up to 50MHz, up to 25 MB/sec
  - **UHS Mode:**
    - SDR12: SDR up to 25MHz, 1.8V signaling
    - SDR25: SDR up to 50MHz, 1.8V signaling
    - SDR50: 1.8V signaling, frequency up to 100MHz, up to 50 MB/sec
    - SDR104: 1.8V signaling, frequency up to 208MHz, up to 104MB/sec
    - DDR50: 1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50 MB/sec

    NOTES: 1. Timing in 1.8V signaling is different from that of 3.3V signaling.
    2. To properly run the UHS mode, please ensure the device supports UHS-I mode.
    3. To properly run the PCIe mode, please ensure the device supports PCIe mode.
- **Copyrights Protection Mechanism:** Non-CPRM
- **Support Hot Plug:** Card removal during operating will never harm the content
- **Password Protection of cards (optional & SD mode only):** CMD42-LOCK-UNLOCK
- **Support SD SPI mode**
- **Designed for read intensive and write intensive cards**
- **Electrostatic Discharge(ESD):**
  - ESD protection in pads (contact discharge).
  - ESD protection in non-contact pad area (air discharge).
- **Operation voltage range:**
  - VDD1: 2.7V~3.6V, VDD2: 1.70V~1.95V

- **Temperature Range:**
  - Commercial grade operation Temp. Range: -25℃~85℃ (Tc 95C)
  - Storage Temp. Range: -40℃~85℃
- **Compliant Specifications - SD Memory Card Specifications:**
  - Compliant with Part 1 Physical Layer Specification Ver. 7.10
  - Compliant with Part 2 File System Specification Ver. 7.00
  - Compliant with Part 3 Security Specification Ver. 7.00
  - Standard Size SD Card Mechanical Addendum Ver. 8.00
- **Certificate:**
  - CE, FCC, BSMI, VCCI

3. ELECTRICAL INTERFACE OUTLINES

3.1. Pad Assignment and Descriptions

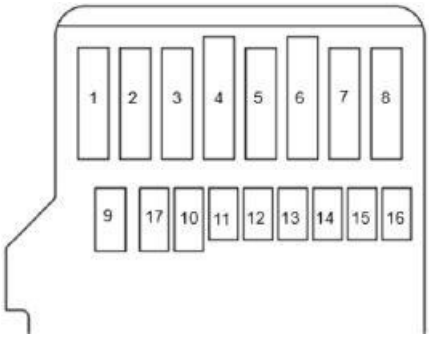


Table 3-1 1-Lane microSD Express Interface Card Pad Assignment

pin	SD Mode			PCIe Mode		
	Name	Type(1)	Description	Name	Type	Description
1	DAT2	I/O	Data Line	DAT2/CLKREQ#	I/O	Data Line/Reference clock request signal.
2	CD/DAT3	I/O	Card Detect/Data Line	CD/DAT3/PERST#	I/O	Card Detect/Data Line/Power Enable Reset
3	CDM	I/O	Command/Response	CMD	I/O	Command/Response
4	VDD	S	Supply voltage (3.3V)	VDD1	S	Supply voltage (3.3V)
5	CLK	I	Clock	CLK	I	Clock
6	VSS	S	Supply voltage ground	VSS	S	Supply voltage ground
7	DAT0	I/O	Data Line	DAT0/REFCLK+	I/O	Data Line/PCIe Ref Clock
8	DAT1	I/O	Data Line	DAT1/REFCLK-	I/O	Data Line/PCIe Ref Clock
9	-	-	Not Used	VDD2	S	Supply voltage (1.8V)
10	-	-	Not Used	VSS	S	Supply voltage ground
11	-	-	Not Used	PCIe TX+	I	PCIe Transmit lane
12	-	-	Not Used	PCIe TX-	I	PCIe Transmit lane
13	-	-	Not Used	VSS	S	Supply voltage ground
14	-	-	Not Used	PCIe RX-	O	PCIe Receive Lane
15	-	-	Not Used	PCIe RX+	O	PCIe Receive Lane
16	-	-	Not Used	VSS	S	Supply voltage ground
17	-	-	Not Used		-	Not Used

(1) S: power supply, I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers; OD: I/O using Open Drain drivers; IDS: Input Differential Signal; ODS: Output Differential Signal

(2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode as well while

they are not used. It is defined so in order to keep compatibility to MultiMedia Cards.

(3) At power up, this line has a 50KOhm pull up enabled in the card. This resistor serves two functions: Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode, it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user during regular data transfer with SET_CLR_CARD_DETECT (ACMD42) command.

(3) Pin2 and Pin5 shall not be kept open by host in PCIe Mode.

3.2. PCIe Bus

Refer to PCI Express standard defined by the PCI-SIG. The command layer used by the PCIe interface is NM Express(NVMe) and standard defined by the NVM Express.

3.3. microSD Card Bus Topology

The microSD card supports 2 alternative communication protocols, SD and SPI BUS mode.
Host can choose either one of both bus mode, same data can be read or written by both modes.
SD mode allows 4-bits data transfer way, it provides high performance. SPI mode supports 1-bit data transfer and of course the performance is lower compared to SD mode.

3.4. microSD Bus Mode Protocol

In default speed, the microSD Memory Card bus has a single master (application); multiple slaves (Cards), synchronous star topology (refer to Figure 3-2). In high speed and UHS-I, the SD Memory Card bus has a single master (application) and single slave (card), synchronous point to point topology. Clock, power and ground signals are common to all cards. Command (CMD) and data (DAT0-DAT3) signals are dedicated to each card providing continues point to point connection to all the cards.
During initialization process commands are sent to each card individually, allowing the application to detect the cards and assign logical addresses to the physical slots. Data is always sent (received) to (from) each card individually. However, in order to simply the handling of the card stack, after the initialization process, all commands may be sent concurrently to all cards. Addressing information is provided in the command packet.
SD bus allows dynamic configuration of the number of data lines. After power up, by default, the SD Memory Card will use only DAT0 for data transfer. After initialization the host can change the bus width (number of data active lines). This feature allows easy tradeoff between HW cost and system performance. Note that while DAT1 to DAT3 are not in use, the related Host's DAT lines should be in tri-state (input mode).

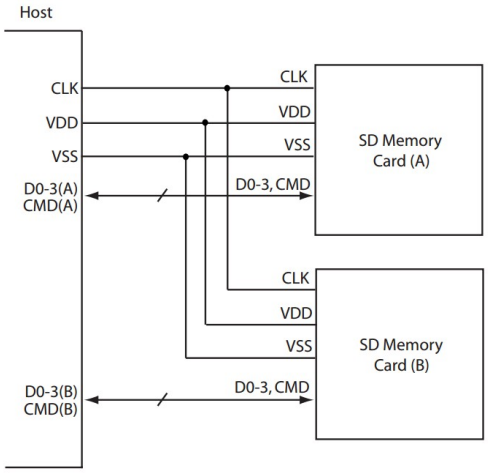


Figure 3-2 microSD Memory Card System Bus Topology

The SD bus includes the following signals:

CLK: Host to card clock signal

CMD: Bidirectional Command/Response signal

DAT0-DAT3: 4 Bidirectional data signals

V_{DD}, V_{ss1}, V_{ss2}: Power and ground signals

Table 3-2 SD Mode Command Set

Card Command Class (CCC)	0 basic	1 Command Queue	2 block read	3 reserved	4 block write	5 erase	6 write protec-tion	7 lock card	8 application specific	9 I/O mode	10 switch	11 extension
CMD0	+											
CMD2	+											
CMD3	+											
CMD4	+											
CMD5										+		
CMD6											+	
CMD7	+											
CMD8	+											
CMD9	+											
CMD10	+											
CMD11	+											
CMD12	+											
CMD13	+											
CMD15	+											
CMD16			+		+			+				
CMD17			+									
CMD18			+									
CMD19			+									
CMD20			+		+							
CMD21												+
CMD23			+		+							
CMD24					+							
CMD25					+							
CMD27					+							
CMD28							+					
CMD29							+					
CMD30							+					
CMD32						+						
CMD33						+						
CMD34-37											+	
CMD38						+						
CMD40								+				
CMD42								+				
CMD43-47		+										
CMD48												+
CMD49												+
CMD50											+	
CMD52										+		
CMD53										+		

Card Command Class (CCC)	0 basic	1 Command Queue	2 block read	3 reserved	4 block write	5 erase	6 write protec-tion	7 lock card	8 application specific	9 I/O mode	10 switch	11 extension
CMD55									+			
CMD56									+			
CMD57											+	
CMD58												+
CMD59												+
ACMD6									+			
ACMD13									+			
ACMD14									+			
ACMD15									+			
ACMD16									+			
ACMD22									+			
ACMD23									+			
ACMD28									+			
ACMD41									+			
ACMD42									+			
ACMD51									+			

Commands	Support requirements
CMD0	Mandatory
CMD2	Mandatory
CMD3	Mandatory
CMD4	Mandatory
CMD5	Optional
CMD6	Mandatory for cards version 1.10 and after
CMD7	Mandatory
CMD8	Mandatory for cards version 2.00 and after
CMD9	Mandatory
CMD10	Mandatory
CMD11	Mandatory for cards supporting UHS-I. Optional for cards that do not support UHS-I.
CMD12	Mandatory
CMD13	Mandatory
CMD15	Mandatory
CMD16	Mandatory
CMD17	Mandatory
CMD18	Mandatory
CMD19	Mandatory for cards supporting UHS-I. Optional for cards that do not support UHS-I.

Commands	Support requirements
CMD20	Not supported for SDSC cards. Mandatory for SDHC and SDXC cards that support Video Speed Class. Optional for SDHC cards that support: a) Speed Class; or b) UHS Speed Grade, and do not support Video Speed Class. Mandatory for SDXC cards that support Speed Class or UHS Speed Grade.
CMD21	Optional
CMD23	Not supported for SDSC cards. Mandatory for SDHC and SDXC cards that support UHS104. Optional for SDHC and SDXC cards that do not support UHS104.
CMD24	Mandatory for writable types of cards
CMD25	Mandatory for writable types of cards
CMD27	Mandatory for writable types of cards
CMD28	Optional
CMD29	Optional
CMD30	Optional
CMD32	Mandatory for writable types of cards
CMD33	Mandatory for writable types of cards
CMD34-37	Optional for cards version 1.10 and after
CMD38	Mandatory for writable types of cards Discard and FULE support is optional
CMD40	Optional
CMD42	Optional for cards version 1.01 and 1.10. Mandatory for cards version 2.00 and after. COP support is optional for CMD42
CMD43-47	Mandatory for cards supporting Command Queue
CMD48	Optional Mandatory for cards supporting Performance Enhancement functions (refer to 5.8.2)
CMD49	Optional Mandatory for cards supporting Performance Enhancement functions (refer to 5.8.2)
CMD50	Optional for cards version 1.10 and after
CMD52	Optional
CMD53	Optional
CMD55	Mandatory
CMD56	Mandatory
CMD57	Optional for cards version 1.10 and after
CMD58	Optional
CMD59	Optional
ACMD6	Mandatory
ACMD13	Mandatory
ACMD14	Optional
ACMD15	Optional
ACMD16	Optional
ACMD22	Mandatory for writable types of cards
ACMD23	Mandatory for writable types of cards
ACMD28	Optional
ACMD41	Mandatory
ACMD42	Mandatory
ACMD51	Mandatory

3.5. SPI Bus Mode Protocol

While the microSD Memory Card channel is based on command and data bit streams that are initiated by a start bit and terminated by a stop bit, the SPI channel by byte oriented. Every command or data block is built for 8-bit bytes and is byte aligned with the CS signal (i.e. the length is a multiple of 8 clock cycles). The card starts to count SPI bus clock cycle at the assertion of the CS signal. Every command or data token shall be aligned with 8-clock cycle boundary.

Similar to the SD Memory Card Protocol, the SPI messages consist of command, response and data-block tokens.

The advantage of SPI mode is reducing the host design effort, especially for MMC host side, it just be modified by little change. Note: please use SD card specification to implement SPI mode function, not use MMC specification. For example, SPI mode is initialized by ACMD41, and the registers are different from MMC card, especially CSD register.

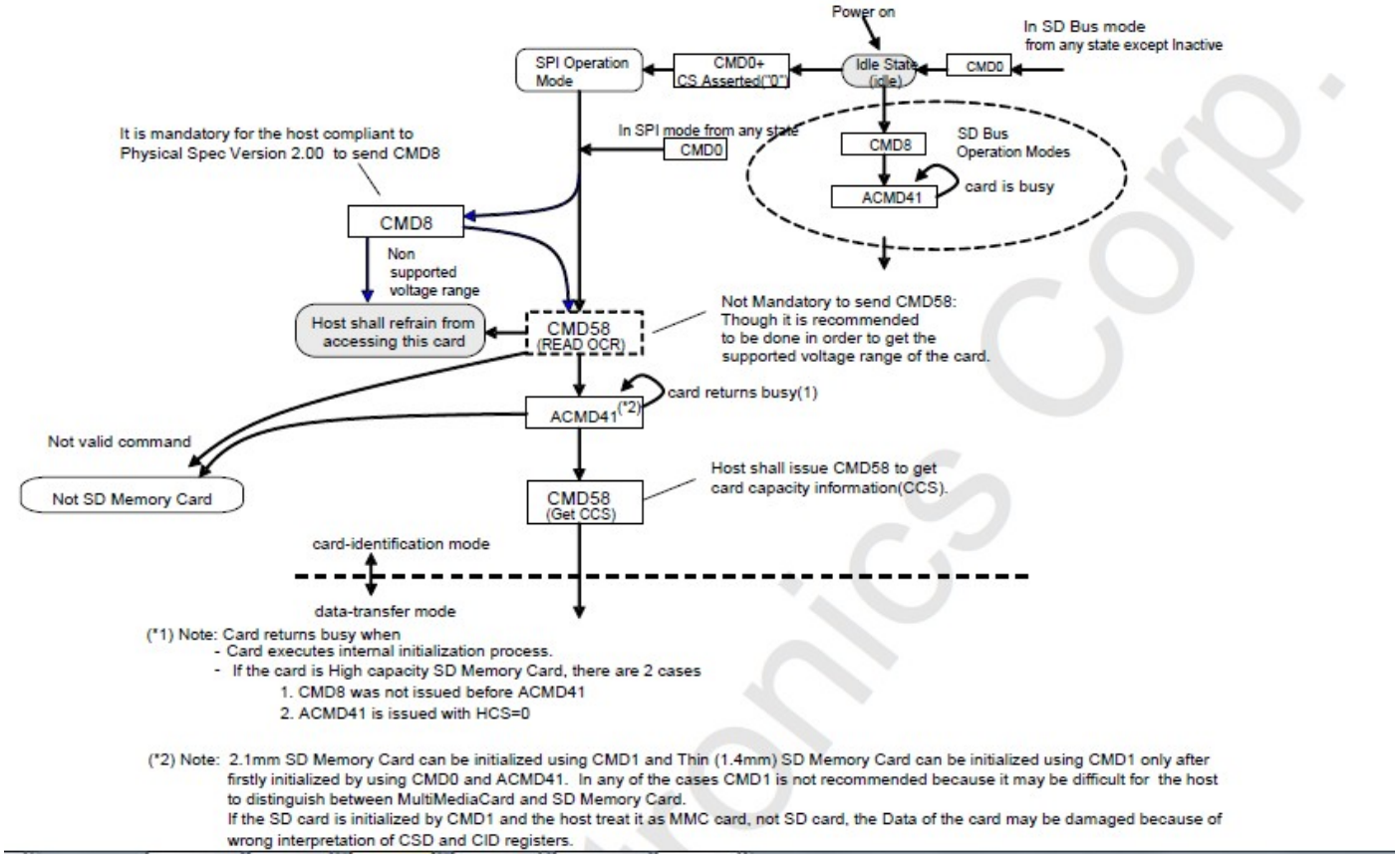


Figure 3-3 SD Memory Card State Diagram (SPI mode)

Table 3-3 SPI Mode Command Set

Card Command Class (CCC)		0	1	2	3	4	5	6	7	8	9	10	11
Supported commands	class description	basic	reserved	block read	reserved	block write	erase	write protection	lock card	application specific	I/O mode	switch	reserved
CMD0	Mandatory	+											
CMD1	Mandatory	+											
CMD5	Optional										+		
CMD6[2]	Mandatory											+	
CMD8[3]	Mandatory	+											
CMD9	Mandatory	+											
CMD10	Mandatory	+											
CMD12	Mandatory	+											
CMD13	Mandatory	+											
CMD16	Mandatory			+		+			+				
CMD17	Mandatory			+									
CMD18	Mandatory			+									
CMD24	Mandatory[1]					+							
CMD25	Mandatory[1]					+							

Card Command Class (CCC)		0	1	2	3	4	5	6	7	8	9	10	11
Supported commands	class description	basic	reserved	block read	reserved	block write	erase	write protection	lock card	application specific	I/O mode	switch	reserved
CMD27	Mandatory[1]					+							
CMD28	Optional							+					
CMD29	Optional							+					
CMD30	Optional							+					
CMD32	Mandatory[1]						+						
CMD33	Mandatory[1]						+						
CMD34-37[2]	Optional											+	
CMD38	Mandatory[1]						+						
CMD42[4]	(Note 4)								+				
CMD50[2]	Optional											+	
CMD52	Optional										+		
CMD53	Optional										+		
CMD55	Mandatory									+			
CMD56	Mandatory									+			
CMD57[2]	Optional											+	
CMD58	Mandatory	+											
CMD59	Mandatory	+											
ACMD13	Mandatory									+			
ACMD22	Mandatory[1]									+			
ACMD23	Mandatory[1]									+			
ACMD41	Mandatory									+			
ACMD42	Mandatory									+			
ACMD51	Mandatory									+			

Note (1): The commands related write and erase are mandatory only for the Writable types of Cards.
Note (2): This command was defined in spec version 1.10
Note (3): This command is newly defined in version 2.00
Note (4): This command is optional in Version 1.01 and 1.10 and mandatory from Version 2.00. COP support is optional for CMD42

3.6. microSD card initialization

PCIe mode:

There are two options for microSD Express initialization, one is starting with issuing SD commands, and the other is without issuing SD commands. KODAK microSD Express card support both types of initialization. Starting with issuing SD commands is recommended by SDA because it can detect card type properly by SD CMD8 and avoid any unexpected compatibility issues.

- **SD initialization sequence starting by SD commands with HVS** (Host and card both do not support VDD3)

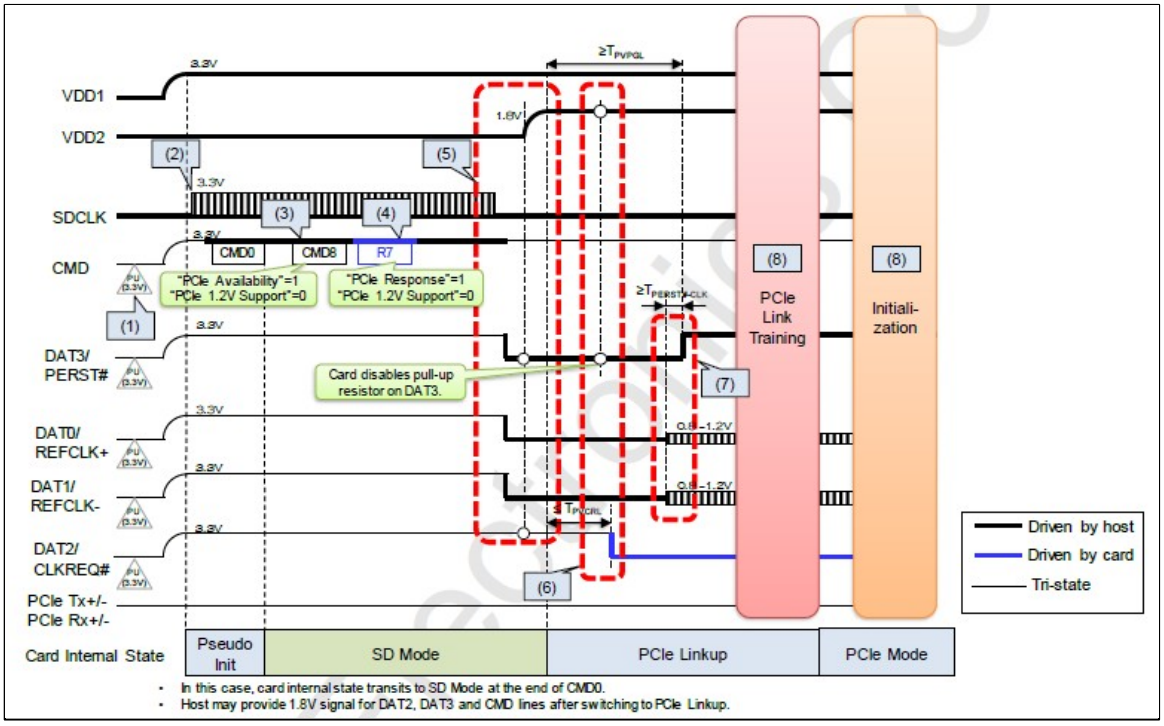


Figure 3-5 Initialization Starts from SD CMD8 by HVS

(1) Before VDD1 power supply, SD Experss Host pulls up CMD and DAT[3:0] lines by 3.3V.
(2) After VDD1 is supplied, the Host supplies SDCLK, and issues CMD0.
(3) The Host issues CMD8 with "PCIe Availability"=1 and "PCIe 1.2V Support"=0 in its argument, because it does not support VDD3.
(4) SD Express Card receives the CMD8 and detects "PCIe Availability"=1 and "PCIe 1.2V Support"=0 successfully. In this case, it responds R7 with "PCIe Response"=1 and "PCIe 1.2V Support"=0. Note that even if the Card supports VDD3, it shall always respond R7 with "PCIe 1.2V Support"=0 when it receives CMD8 with "PCIe 1.2V Support"=0.
(5) When the Host detects "PCIe Response"=1 in R7, it drives DAT3 (PERST#), DAT0 (REFCLK+) and DAT1 (REFCLK-) Low. And the Host supplies VDD2.
(6) When the card detects VDD2 on and PERST#=Low, it disables its internal pull-up resistor on DAT3, then it drives CLKREQ# (DAT2) Low within T_{PVCRL} from VDD2 stabilization.
(7) When the Host detects CLKREQ#=Low, it drives PERST# (DAT3) High after more than T_{PVPGL} from VDD2 stabilization and more than $T_{PERST\#-CLK}$ from supplying REFCLK via DAT0 and DAT1 lines.
(8) The Host executes PCIe Link Training and initialization.

■ **SD initialization sequence starting by direct PCIE**

When host and card does not support VDD3, host can supply VDD2 instead of VDD3 just after VDD1 is on. Meaning VDD3 is substituted to VDD2.

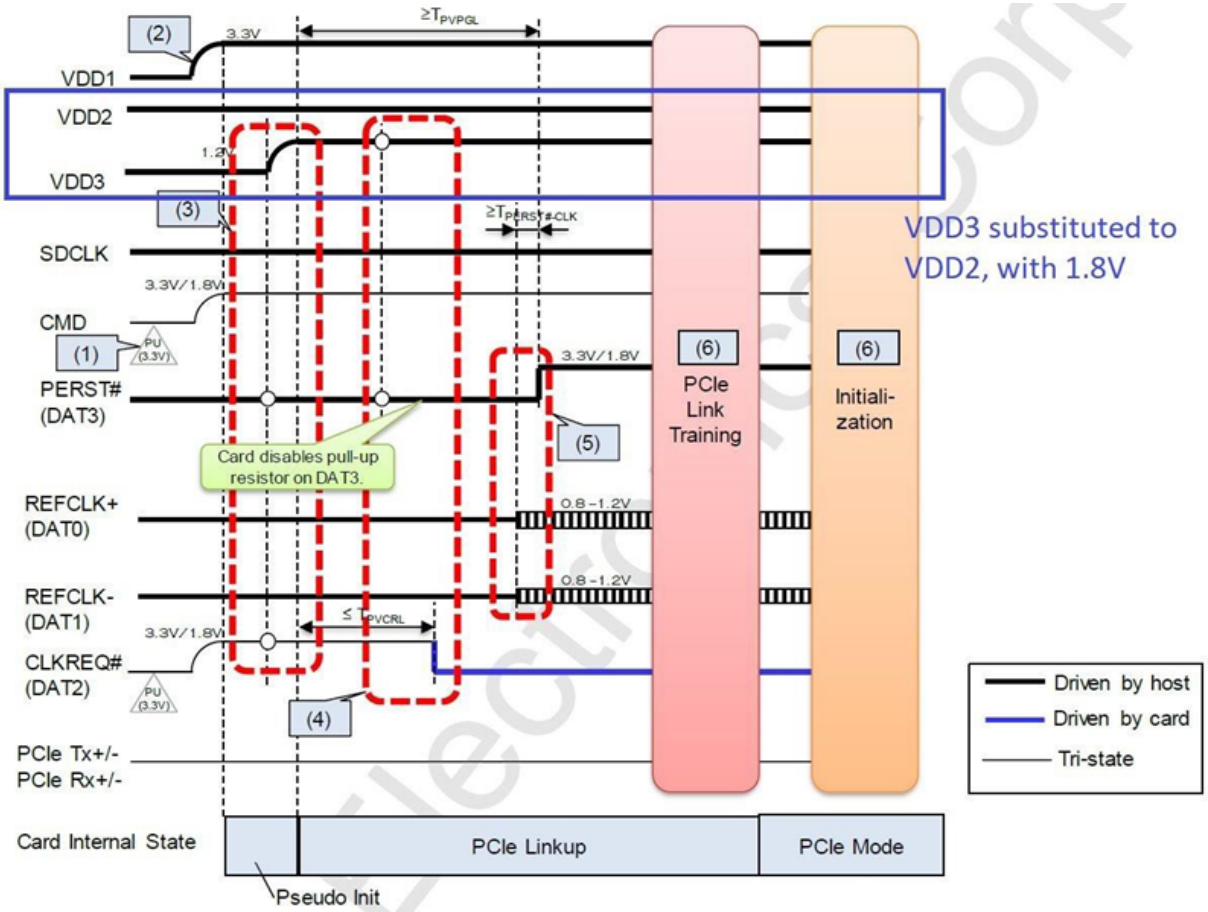


Figure 3-6 Direct PCIe Initialization

(1) Before VDD1 power supply, SD Express Host drives SDCLK, PERST# (DAT3), REFCLK (DAT0 and DAT1) Low, and pulls up CLKREQ# (DAT2) and CMD by 3.3V.
(2) The Host supplies VDD1.
(3) After that, if the Host detects PERST#=Low and CLKREQ#=High, it supplies VDD3.
(4) When the card detects VDD3 on and PERST#=Low, it disables its internal pull-up resistor on DAT3, then it drives CLKREQ# (DAT2) Low within T_{PVCRL} from VDD3 stabilization.
(5) When the Host detects CLKREQ#=Low, it drives PERST# (DAT3) High after more than T_{PVPGL} from VDD3 stabilization and more than $T_{PERST\#-CLK}$ from supplying REFCLK via DAT0 and DAT1 lines.
(6) The Host executes PCIe Link Training and initialization.

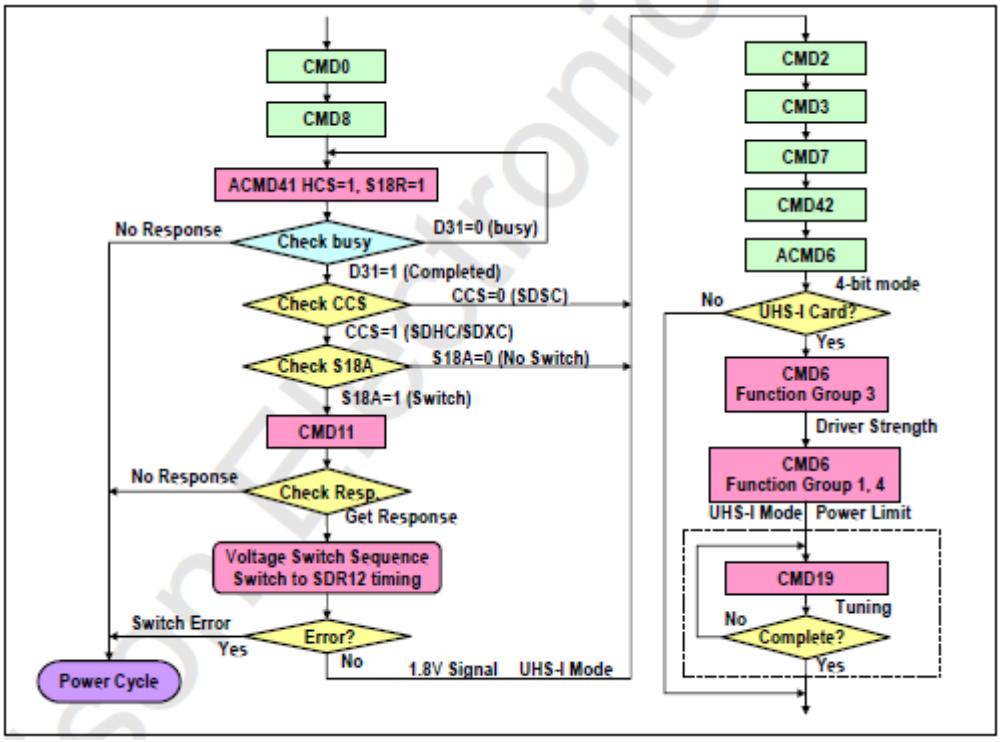


Figure 3-7 UHS-I Host Initialization Flow Chart

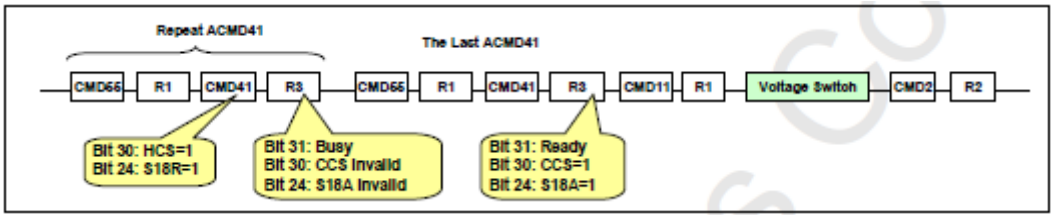


Figure 3-8 ACMD41 Timing Followed by Voltage Switch Sequence

When signaling level is 3.3V, host repeats to issue ACMD41 with HCS=1 and S18R=1 until the response indicates ready. The argument (HCS and S18R) of the first ACMD41 is effective but the all following ACMD41 should be issued with the same argument.

If Bit31 indicates ready, host needs to check CCS and S18A.

The card indicates S18A=0, which means that voltage switch is not allowed and the host needs to use current signaling level.

Table 3-4 S18R and S18A Combinations

Current Signaling Level	S18R	S18A	Comment
3.3V	0	0	1.8V signaling is not requested
	1	0	The card does not support 1.8V signaling
	1	1	Start signal voltage switch sequence
1.8V	X	0	Already switched to 1.8V

To change signaling level at the same time between host and card, signal voltage switch sequence is invoked by CMD11 as shown in Figure 3-6. CMD11 is issued only when S18A=1 in the response of ACMD41.

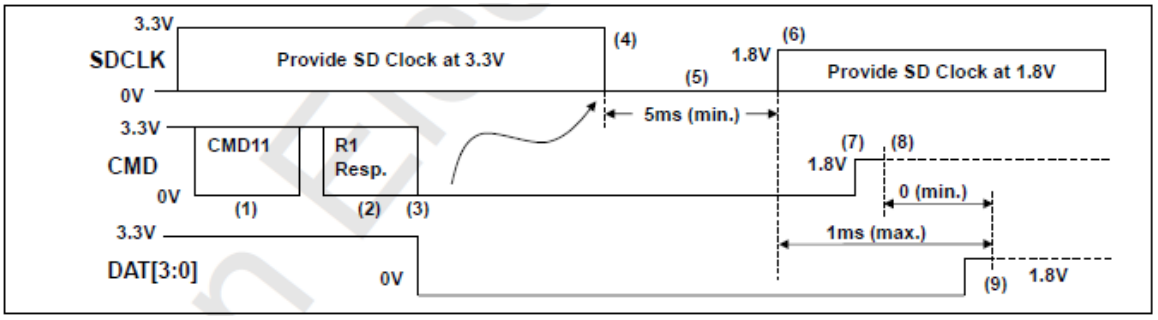


Figure 3-9 Signal Voltage Switch Sequence

4. ENVIRONMENTAL SPECIFICATIONS

4.1. Environmental Conditions

Temperature range

- Temperature Range
  - Operational: -25°C ~ 85°C (Tc 95°C)
  - Storage: -40°C ~ 85°C

High Temperature Test Condition

	Temperature	Humidity	Test Time
Operation (C-grade)	85°C	0% RH	96 hours
Storage	85°C	0% RH	500 hours

Low Temperature Test Condition

	Temperature	Humidity	Test Time
Operation (C-grade)	-25°C	0% RH	96 hours
Storage (C-grade)	-40°C	0% RH	168 hours

High Humidity Test Condition

	Temperature	Humidity	Test Time
Operation (C-grade)	25°C	95% RH	1 hours
Storage (C-grade)	40°C	93% RH	500 hours

Temperature Cycle Test

	Temperature	Test Time	Cycle
Operation (C-grade)	-25°C	30 min	10 cycles
	85°C	30 min	
Storage	-40°C	30 min	50 Cycles
	85°C	30 min	

Shock Specification

	Acceleration Force	Half Sin Pulse Duration
Commercial grade	500G	1ms

Vibration Specification

	Condition		Vibration Orientation
	Frequency/Displacement	Frequency/Acceleration	
microSD card	20Hz~80Hz/1.52mm	80Hz~2000Hz/20G	X, Y, Z axis/30 min for each

Drop Specification

	Height of Drop	Number of Drop
microSD card	150cm free fall	6 face of each unit

Bending Specification

	Force	Action
microSD card	≥ 10N	Hold 1min/5times

Torque Specification

	Force	Action
microSD card	0.1N-m or +/-2.5 deg	Hold 30 seconds/5times

Salt Spray Specification

	Condition	Action
microSD card	Concentration: 3% NaCl Temperature: 35℃	Storage for 24 HRS

Waterproof Specification

	Condition	Action
microSD card	Water temperature: 25℃ Water depth: The lowest point of unit is locating 1000mm below surface.	Storage for 30 mins

IPX7 compliance

X-Ray Exposure Specification

	Condition	Action
microSD card	0.1 Gy of medium-energy radiation (70 keV to 140 keV, cumulative dose per year) to both sides of the card	Storage for 30 mins

ISO 7816-1 compliance

Durability Test

	Mating cycle
microSD card	10000 times

Contact ESD Specification

	Condition
microSD card	Contact: +/- 4KV each item 25 times Air: +/- 8KV 10 times

EMI Compliance

- FCC: CFR47 Part15 Subpart B Class B
- CE: EN55032, EN55035
- BSMI: CN13438
- VCCI: CISPR 32

5. SD CARD COMPARISON

Table 5-1 Comparing SDSC, SDHC, and SDXC

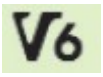
	SDSC	SDHC	SDXC
File System	FAT 12/16	FAT32	exFAT
Addressing Mode	Byte (1 byte unit)	Block (512 byte unit)	Block (512 byte unit)
HCS/CCS bits of ACMD41	Support	Support	Support
CMD8 (SEND_IF_COND)	Support	Support	Support
CMD16 (SET_BLOCKLEN)	Support	Support (Only CMD42)	Support (Only CMD42)
Partial Read	Support	Not Support	Not Support
Lock/Unlock Function	Mandatory	Mandatory	Mandatory
Write Protect Groups	Optional	Not Support	Not Support
Supply Voltage 2.7v – 3.6v (for operation)	Support	Support	Support
Total Bus Capacitance for each signal line	40pF	40pF	40pF
CSD Version (CSD_STRUCTURE Value)	1.0 (0x0)	2.0 (0x1)	2.0 (0x1)
Speed Class	Optional	Mandatory (Class 2 / 4 / 6 / 10)	Mandatory (Class 2 / 4 / 6 / 10)

Table 5-2 Comparing UHS Speed Grade Symbols

	U1 (UHS Speed Grade 1)	U3 (UHS Speed Grade 3)
Operable Under	*UHS-I Bus I/F, UHS-II Bus I/F	
SD Memory Card	SDHC UHS-I and UHS-II, SDXC UHS-I and UHS-II	
Mark		
Performance	10 MB/s minimum write speed	30 MB/s minimum write speed
Applications	Full higher potential of recording real-time broadcasts and capturing large-size HD videos.	Capable of recording 4K2K video.

*UHS (Ultra High Speed), the fastest performance category available today, defines bus-interface speeds up to 312 Megabytes per second for greater device performance. It is available on SDXC and SDHC memory cards and devices.

Table 5-3 Comparing Video Speed Class Symbols

	V6	V10	V30	V60	V90
Bus Speed Mode Requirement	Non UHS UHS-I UHS-II	Non UHS UHS-I UHS-II	Non UHS UHS-I UHS-II	UHS-II	UHS-II
Card Capacity	SDHC, SDXC				
Mark					
Performance (Minimum Sequential Write Speed)	6MB/s	10MB/s	30MB/s	60MB/s	90MB/s
Applications	Standard Video	Full HD Video HD Video	4K2K Video Full HD Video	4K2K Video	8K Video

6. ELECTRICAL SPECIFICATIONS

6.1 Power Consumption

The table below is the power consumption of SD card with different bus speed modes.

Table 6-1 Power Consumption of microSD card (UHS-I Mode)

Bus Speed Mode		Max. Power Up Current (uA)	Max. Standby Current (uA)	Max. Read Current (mA)	Max. Write Current (mA)
Default Speed Mode		250	1000	150 @ 3.6V	150[3] @ 3.6V
High Speed Mode		250	1000	200 @ 3.6V	200 @ 3.6V
UHS-I Mode	UHS50/DDR50	250	1000	400 @ 3.6V	400 @ 3.6V
	UHS104/DDR50	250	1000	400 @ 3.6V	400 @ 3.6V

NOTES:

1. Power consumptions are measured at room temperature.
2. Power consumption of Max. Standby Current is for SD cards under and including 64GB only. For 128GB and 256GB, the power consumption is to be determined.
3. For SDXC, up to 100mA from VDD1 when XPC=0; up to 150mA from VDD1 when XPC=1.

Table 6-2 Power Consumption of microSD Express (PCIe Gen3x1)

Power Rail	Voltage Tolerance	Current Consumption Limit			
		Peak mA Max Avg @ 100us		Normal mA Max Avg @ 1s	
3.3V	2.7V – 3.6V	VDD1	522	VDD1	421
		VDD2	110	VDD2	100

Notes:

1. Power consumptions are measured at room temperature.
2. Table 6-2 is determined by RMS value.

6.2 Working Rating

Item	Symbol	Parameter	MIN	MAX	Unit
1	T_a	Operating Temperature	-40	+85	℃
2	T_{st}	Storage Temperature	-40	+85	℃

Parameter	Symbol	Min	MAX	Unit
Operating Temperature	T_a	-25	+85	℃
V_{DD} Voltage	V_{DD}	2.7	3.6	V

6.3 DC Characteristic

6.3.1 Bus Operation Conditions

Table 6-3 Threshold Level for High Voltage Range

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75*V_{DD}		V	I_{OH}=-2mA V_{DD} Min
Output Low Voltage	V_{OL}		0.125*V_{DD}	V	I_{OL}=2mA V_{DD} Min
Input High Voltage	V_{IH}	0.625*V_{DD}	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.25*V_{DD}	V	
Power Up Time			250	ms	From 0V to V_{DD} min

Parameter	Symbol	Min	Max.	Unit	Remarks
Peak voltage on all lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

Table 6-5 Threshold Level for Low Voltage Range

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Regulator Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.4	-	V	I_{OH}=-2mA
Output Low Voltage	V_{OL}	-	0.45	V	I_{OL}=2mA
Input High Voltage	V_{IH}	1.27	2.00	V	
Input Low Voltage	V_{IL}	V_{ss}-0.3	0.58	V	

Table 6-6 Input Leakage Current for Low Voltage Range

Parameter	Symbol	Min	Max.	Unit	Remarks
Input Leakage Current		-2	2	uA	DAT3 pull-up is disconnected.

6.3.2 Bus Operation Conditions for PCIe

Table 6-7 Bus Operation Conditions of VDD3

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD2}	1.14	1.3	V	
Capacitance connected to V_{DD2}	C_{c2}	-	2	uF	
Host capacitance recommended for V_{DD3}	C_{h3}	22	-	uF	

6.3.3 Bus Signal Line Load

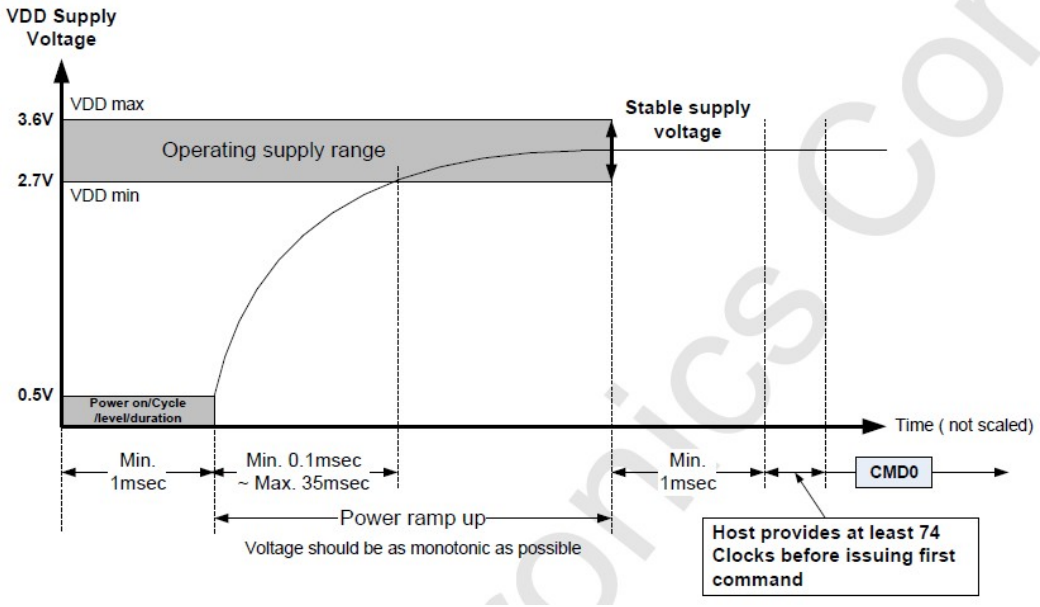
Bus Operation Conditions – Signal Line's Load

Total Bus Capacitance = C_{HOST} + C_{BUS} + N C_{CARD}

Parameter	symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	kΩ	to prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card C_{HOST}+C_{BUS} shall not exceed 30 pF
Card Capacitance for each signal pin	C_{CARD}		10	pF	
Maximum signal line inductance			16	nH	
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	kΩ	May be used for card detection
Capacity Connected to Power Line	C_C		5	uF	To prevent inrush current

6.3.4 Power Up Time of UHS-I Host

The host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.



Power On or Power Cycle

Followings are requirements for Power on and Power cycle to assure a reliable SD Card hard reset.

(1) Voltage level shall be below 0.5V.

(2) Duration shall be at least 1ms.

Power Supply Ramp Up

The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD (min.) and VDD (max.) and host can supply SDCLK.

Followings are recommendations of Power ramp up:

(1) The voltage of power ramp up should be monotonic as much as possible.

(2) The minimum ramp up time should be 0.1ms.

(3) The maximum ramp up time should be 35ms for 2.7-3.6V power supply.

(4) Host shall wait until VDD is stable.

(5) After 1ms VDD stable time, the host provides at least 74 clocks before issuing the first command.

Power Down and Power Cycle

(1) When the host shuts down the power, the card V_{DD} shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.

(2) If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. A power cycle is also needed for accessing cards that are already in *Inactive State.* To create a power cycle the host shall follow the power down description before power up the card (i.e. the card V_{DD} shall be once lowered to less than 0.5Volt for a minimum period of 1ms).

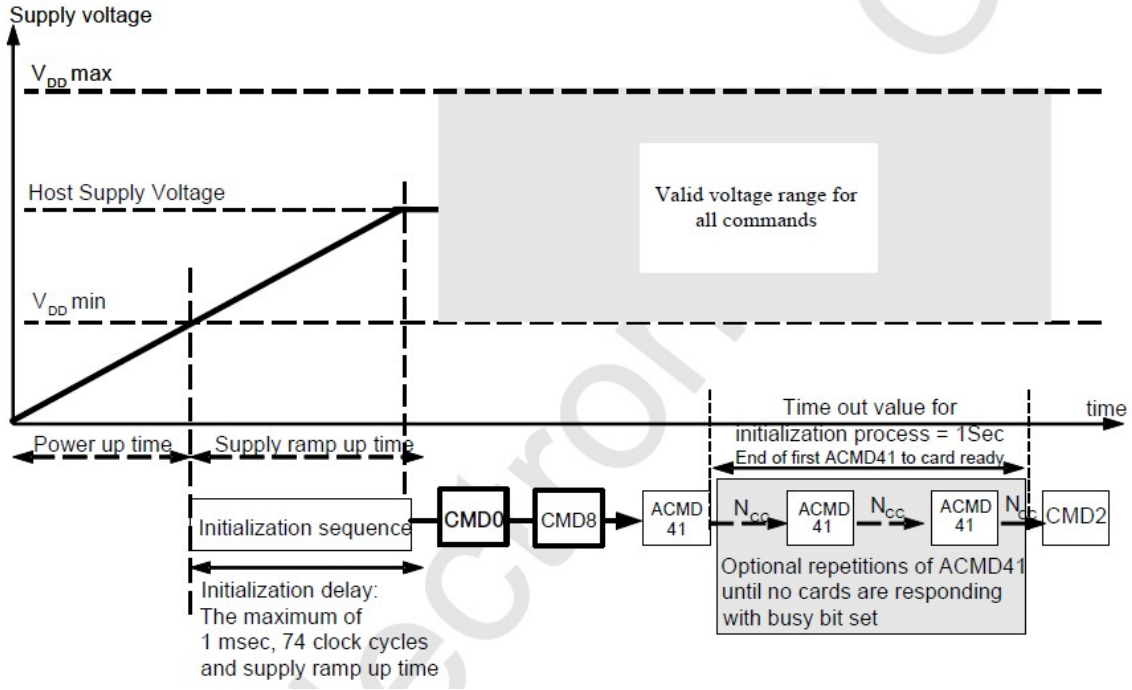
6.3.5 Power Up Sequence of SD Express Host

- Power up and ramp up of VDD1 and VDD2/VDD3 should be monotonic.
- VDD1 shall be supplied first, followed by VDD2/VDD3 if SD Express Card is present.

6.3.5 Power Up Time of UHS-I Card

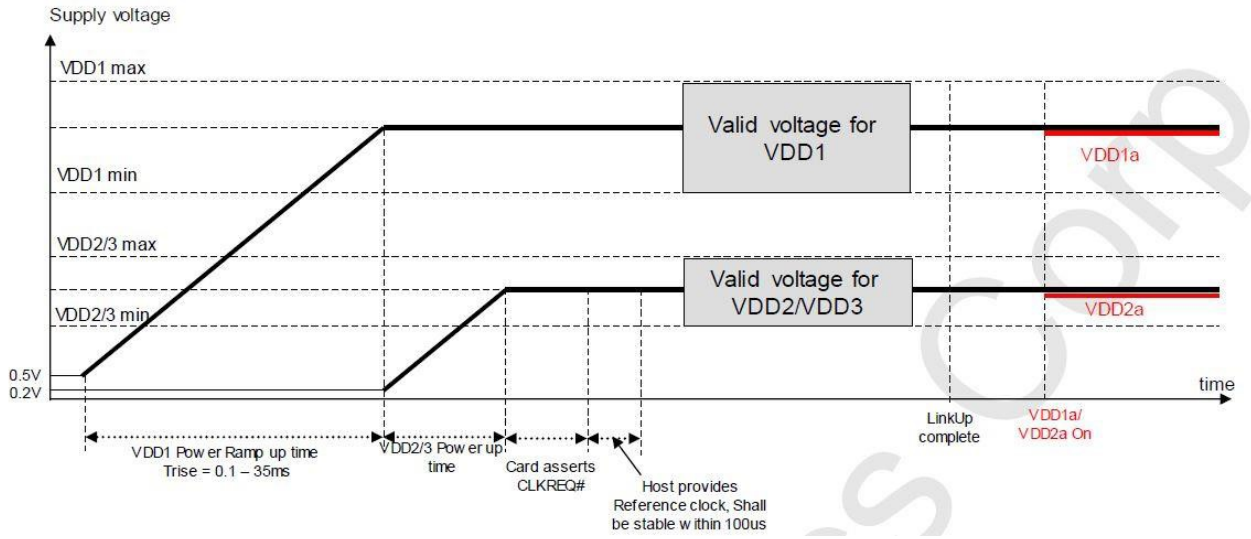
A device shall be ready to accept the first command within 1ms from detecting VDD min.

The device may use up to 74 clocks for preparation before receiving the first command.



Host is recommended to turn on VDD3 only if SD Express Card type presence detected.

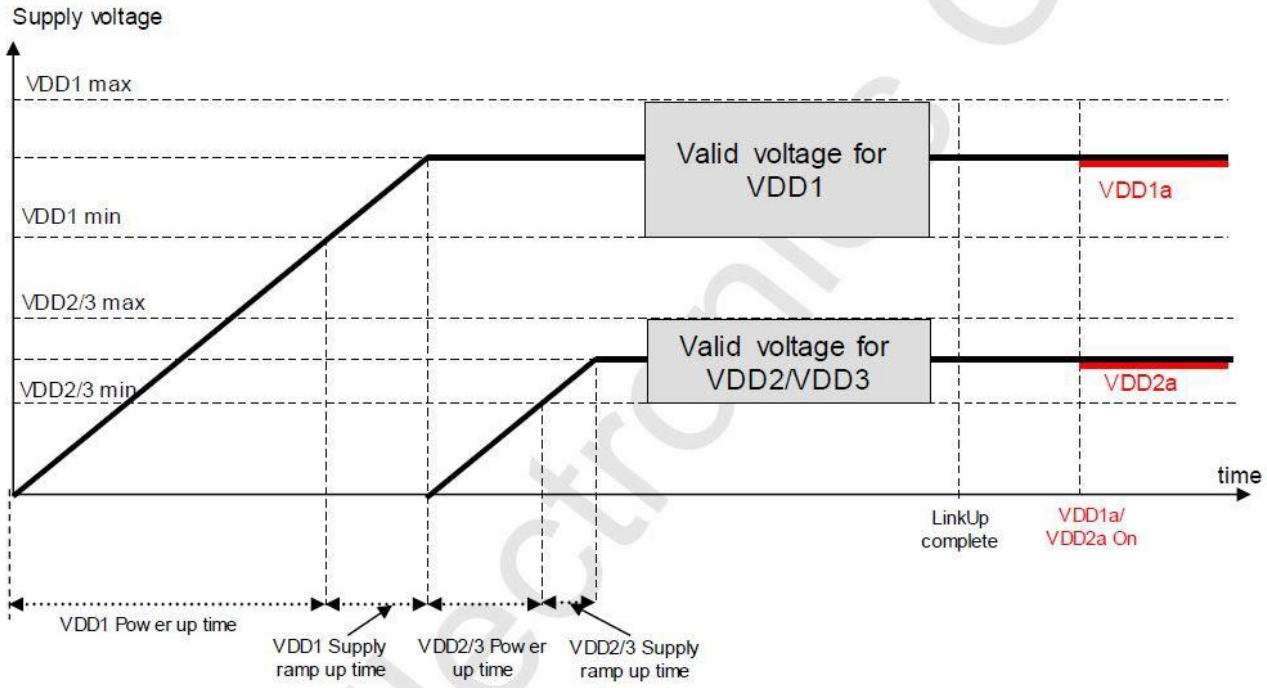
- Trise shall be 0.1-35ms.
- Host shall wait until both VDD1 and VDD2/VDD3 are stable.
- When power cycle is executed, keep VDD1 less than 0.5V and VDD2/VDD3 less than 0.2V at least 1ms before starting power up.



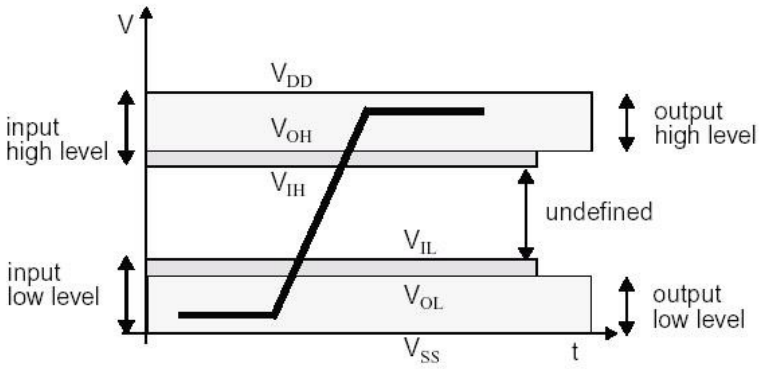
6.3.7 Power Up Sequence of SD Express Card

SD Express card shall support VDD2 (1.8V).

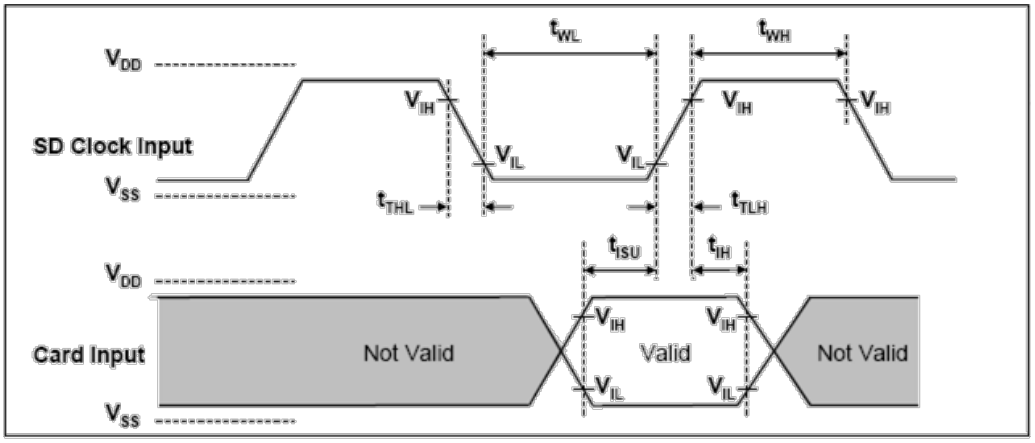
VDD1 shall be supplied first, followed by VDD2 or VDD3 in case that SD Express card presence was detected.



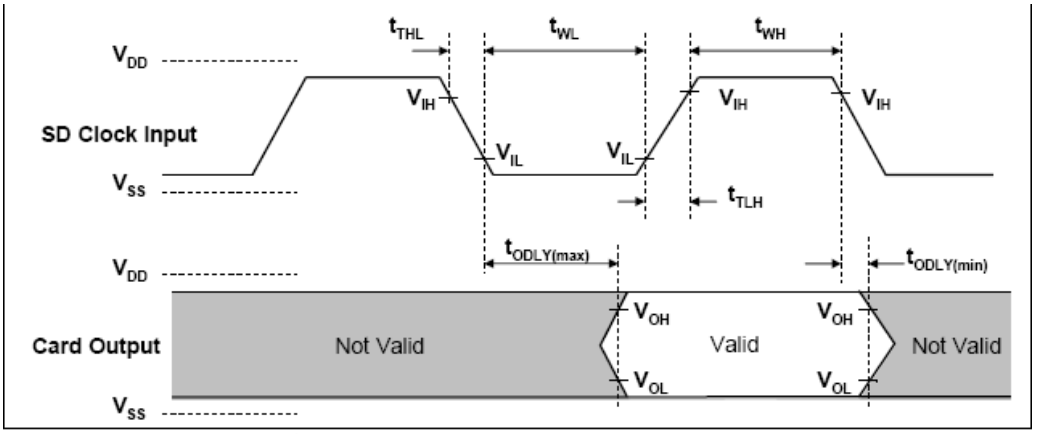
6.4 AC Characteristic



6.4.1 microSD Interface Timing (Default)



Card Input Timing (Default Speed Card)

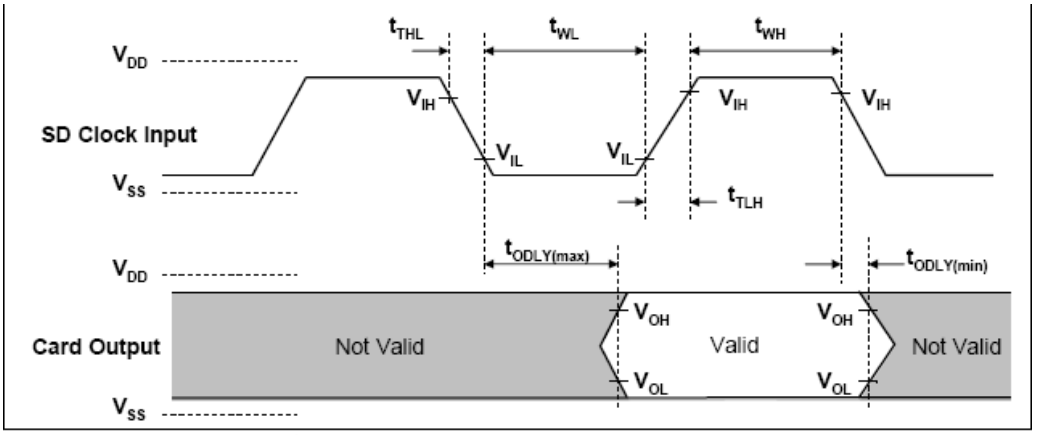


Card Output Timing (Default Speed Mode)

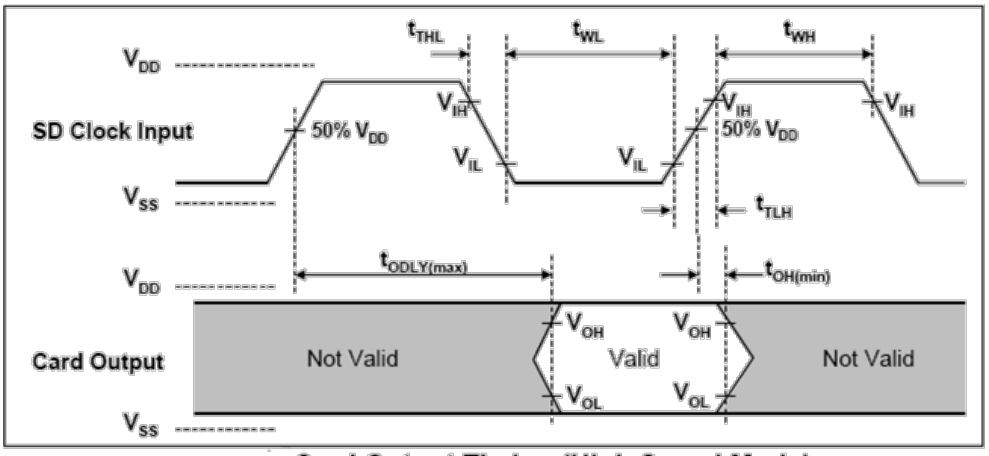
Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	C_{card}≤ 10 pF (1 card)
Clock frequency Identification Mode	f_{OD}	0(1)/100	400	kHz	C_{card}≤ 10 pF (1 card)
Clock low time	t_{WL}	10		ns	C_{card}≤ 10 pF (1 card)
Clock high time	t_{WH}	10		ns	C_{card}≤ 10 pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{card}≤ 10 pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{card}≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	C_{card} ≤ 10 pF (1 card)
Input hold time	t_{IH}	5		ns	C_{card} ≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	C_L ≤ 40 pF (1 card)
Output Delay time during Identification Mode	t_{ODLY}	0	50	ns	C_L ≤ 40 pF (1 card)

(1) 0Hz means to stop the clock. The given minimum frequency range is for cases where continuous clock is required.

6.4.2 microSD Interface Timing (High-Speed Mode)



Card Output Timing (Default Speed Mode)



Card Output Timing (High Speed Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	$C_{card} \leq 10$ pF (1 card)
Clock low time	t_{WL}	7		ns	$C_{card} \leq 10$ pF (1 card)
Clock high time	t_{WH}	7		ns	$C_{card} \leq 10$ pF (1 card)
Clock rise time	t_{TLH}		3	ns	$C_{card} \leq 10$ pF (1 card)
Clock fall time	t_{THL}		3	ns	$C_{card} \leq 10$ pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	$C_{card} \leq 10$ pF (1 card)
Input hold time	t_{IH}	2		ns	$C_{card} \leq 10$ pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	$C_L \leq 40$ pF (1 card)
Output Hold time	t_{OH}	2.5		ns	$C_L \geq 15$ pF (1 card)
Total System capacitance of each line[1]	C_L		40	pF	1 card

(1) In order to satisfy severe timing, the host shall drive only one card.

6.4.3 SD Interface Timing (SDR12, SDR25, SDR50 and SDR104 Modes)

Input

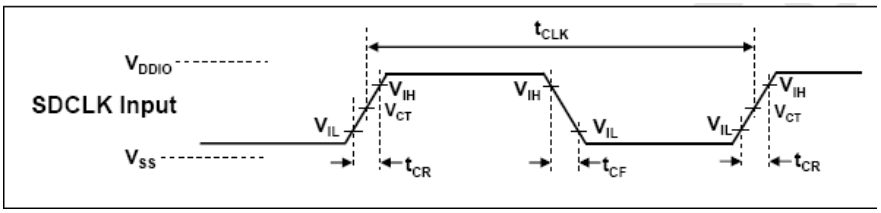
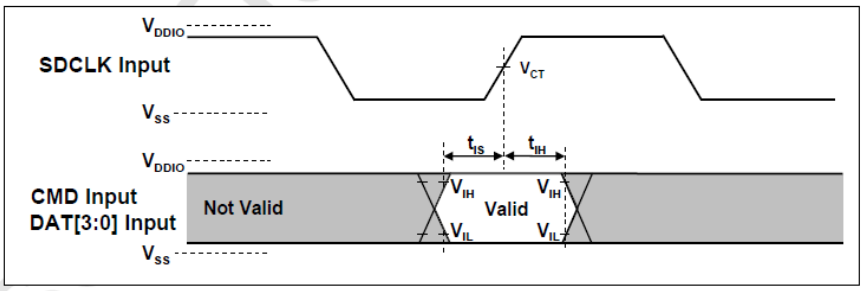


Table 6-8 Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz (Max.), Between rising edge, V_{CT}= 0.975V
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max.) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, C_{CARD}=10pF The maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency
Clock Duty	30	70	%	

SDR12, SDR25, SDR50 and SDR104 Input Timing



Card Input Timing

Symbol	Min	Max	Unit	SDR104 Mode
t_{IS}	1.40	-	ns	C_{CARD} =10pF, V_{CT}= 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT}= 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR12, SDR25 and SDR50 Mode**
t_{IS}	3.00	-	ns	C_{CARD} =10pF, V_{CT}= 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT}= 0.975V

Output(SDR12, SDR25, SDR50)

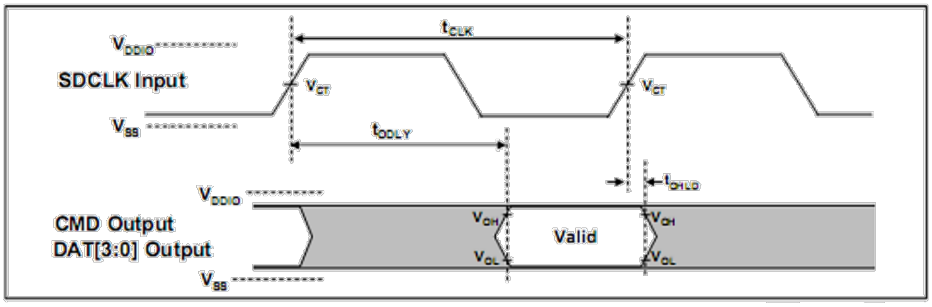


Table 6-9 Output Timing of Fixed Data Window (SDR12, SDR25, SDR50)

Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK}>=10.0ns, C_L=30pF, using driver Type B, for SDR50
t_{ODLY}	-	14	ns	t_{CLK}>=20.0ns, C_L=40pF, using driver Type B, for SDR25 and SDR12,
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.), C_L=15pF

Output(SDR104 Modes)

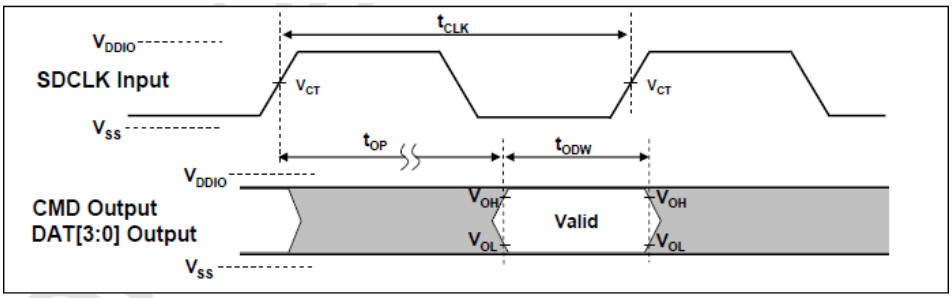
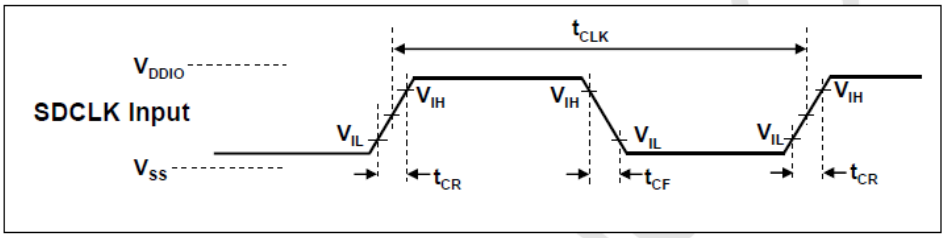


Table 6-10 Output Timing of Variable Window (SDR104)

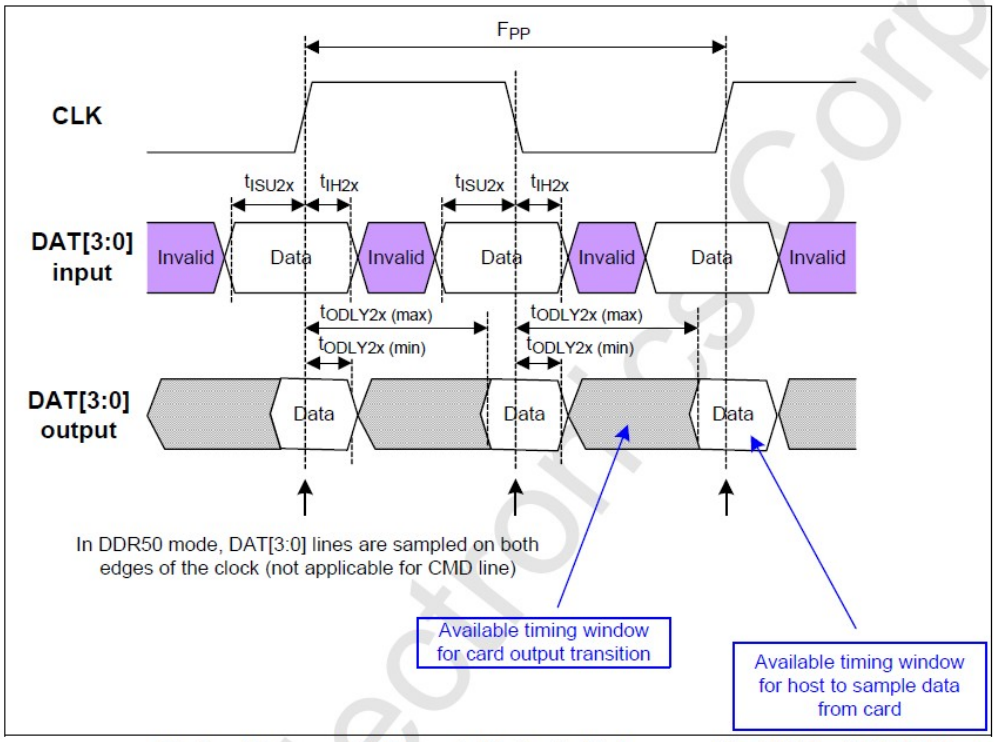
Symbol	Min	Max	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
$\triangle t_{OP}$	-350	+1550	ps	Delay variable due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

6.4.4 SD Interface Timing (DDR50 Mode)



Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max.) at 50MHz, C_{CARD}=10pF
Clock Duty	45	55	%	



Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

Table 6-11 Bus Timings – Parameters Values (DDR50 Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	3	-	ns	$C_{card} \leq 10$ pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}		13.7	ns	$C_L \leq 30$ pF (1 card)
Output Hold time	t_{OH}	1.5	-	ns	$C_L \geq 15$ pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	$C_{card} \leq 10$ pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	$C_L \leq 25$ pF (1 card)
Output Hold time	t_{OH2x}	1.5	-	ns	$C_L \geq 15$ pF (1 card)

7.1 Efficient Data Writing to microSD Memory Card

In order to optimize sequential writing performance and WAF (Write Amplification Factor), it is recommended to use allocation unit (AU) writing.

It is recommended that Multiple_Block_Write shall be used as a command for writing data, and the size of data written by each command should be the FAT cluster x n (n: integer)

7.1.1 Write_Single_Block and Write_Multiple_Block

Write single block (CMD24) was written by one sector (512Bytes), which is suitable to write small area such like updating file system area (FAT). Besides, Write multiple blocks (CMD25) is a command for writing data to blocks that have sequential address per command, which is suitable to write large area such as user data. Write multiple blocks with a cluster unit (512Byte x 128 Sectors = 64KByte) in the file system is an efficient access to the flash memory, it is obviously to provide higher speed to compared to single write block.

And it could be estimated that microSD card internal process would be reduced to save power consumption and flash write amplification factor, that is why the efficient data writing was recommended. To avoid the command issued by 512Bytes with single write block, software processes in the host device become faster. For this operation, check the sectors in the microSD card and file system as Figure 7-1

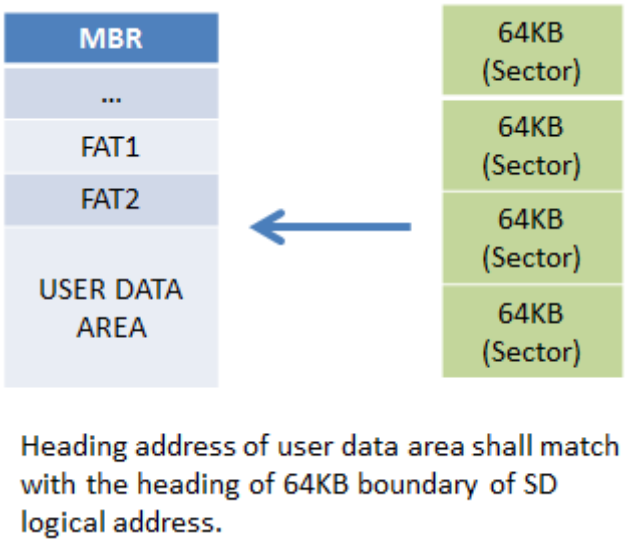


Figure 7-1 Matching between logical address and file system

Note: Large Cluster unit is better for performance and WAF, for example, 128KB, 256KB or 512KB. Large cluster unit also can save write command numbers and few transfer time.

7.2 Basic Process of Error Handling

7.2.1 Retry Process

Execute the process by sending commands again, especially for signal issue between card and host.

7.2.2 Recovery Process

Confirm card status is in Transfer State, if card status is not in Transfer State, please issue Stop command to recover it and execute or continue flow. If there was UECC during read/write status, we could use recovery process to recover it.

7.2.3 Tuning Write Command Process

In order to adjust Host CMD and CLK timing, the way is issue tuning command to confirm what the device response and data was received by host. Based on the response, host was adjusting the timing step by step and recording the pass range. Through this flow host could adjust the appropriate timing settings to avoid unexpected handshaking issue.

7.2.4 Tuning Read Command Process

In order to adjust Host CLK and DAT timing, the way is issue tuning command to confirm what the device response and data was received by host. Based on the response, host was adjusting the timing step by step and recording the pass range. Through this flow host could adjust the appropriate timing settings to avoid unexpected handshaking issue.

7.2.5 Exception Handling Process

No doubt that sometimes we would face all error handling above could not recover it successfully, and we could react based on the situation.

- If there was error in response, we could re-initialize the card.
- If it was signal issue, we could set up signal status by reading data and tuning command.

7.3 Common Error Handling in SPI and SD mode

7.3.1 Time-out

Run the Retry Process. No response from CMD, it might be signal or status got problem. To avoid the infinite loop, implement a retry counter in the host so that, if the retry counter expires, the exception handling starts in the host.

7.3.2 Error Detect (CMD CRC Error)

Run the Recovery Process. If it got second time failure with CRC, the setting might be too margin to receive response stably. Suggestion is use tuning write command to fix timing and then retry it.

7.3.3 Error Detect (Other Error) in SPI and SD mode

Run the Recovery Process.

7.3.4 Others

Most errors could be recovered by running the Recovery Process, let card come into Transfer State and then executing the flow we planned. If it does not work, please use exception method to come back initial state.

7.4 Data Error Handling in SPI and SD mode

7.4.1 Time-out

Run the Recovery Process. While the state was recovered, run the flow again.

7.4.2 Read CRC16 Error

Run the Recovery Process. If it got second time failure with CRC, the setting might be too margin to receive data stably. Suggestion is use tuning read date to fix timing and then retry it.

7.4.3 Write CRC Status Error

Run the Recovery Process. If it got second time failure with CRC, the setting might be too margin to receive CRC status stably. Suggestion is use tuning read date to fix timing and then retry it.

7.4.4 Others

Most errors could be recovered by running the Recovery Process, let card come into Transfer State and then executing the flow we planned.

7.5 Multiple Block Write (CMD25) Process

- If Response is ADDRESS_OUT_OF_RANGE, please confirm writing address.
- If Response is DEVICE_IS_LOCKED, please stop writing data.
- If Response is COM_CRC_ERROR, run retry or tuning.

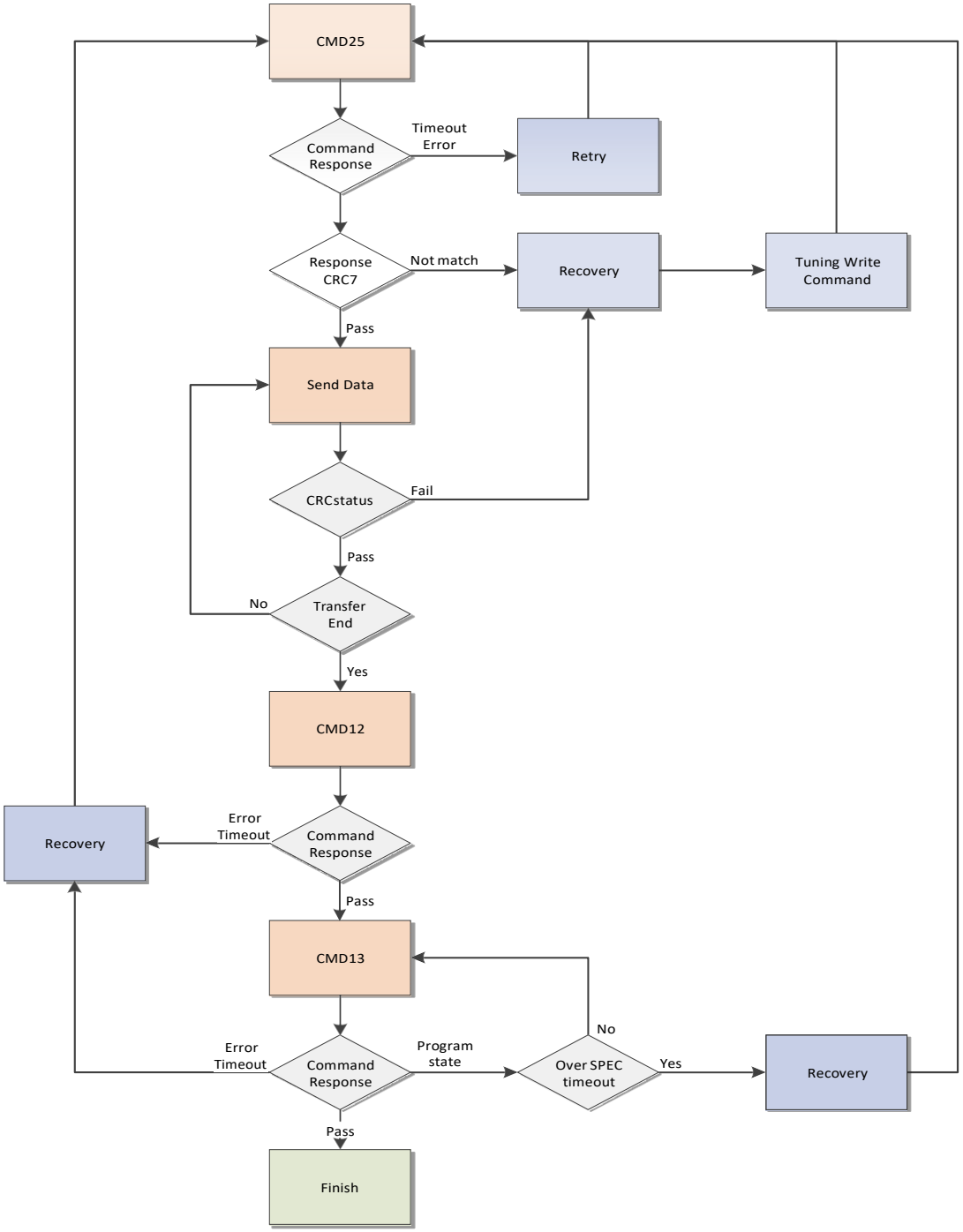


Figure 7-2 Multiple Write (CMD25) Error Handling

7.6 Retry Error handling

In order to avoid signal issue caused unexpected response from device, we could use Retry Process to fix it.

- Please make sure card state is in transfer state before issuing following commands.
- To avoid the infinite loop, implement a retry counter in the host.
- If the device could not respond to CMD13 normally, please runexception handling to recover card status.

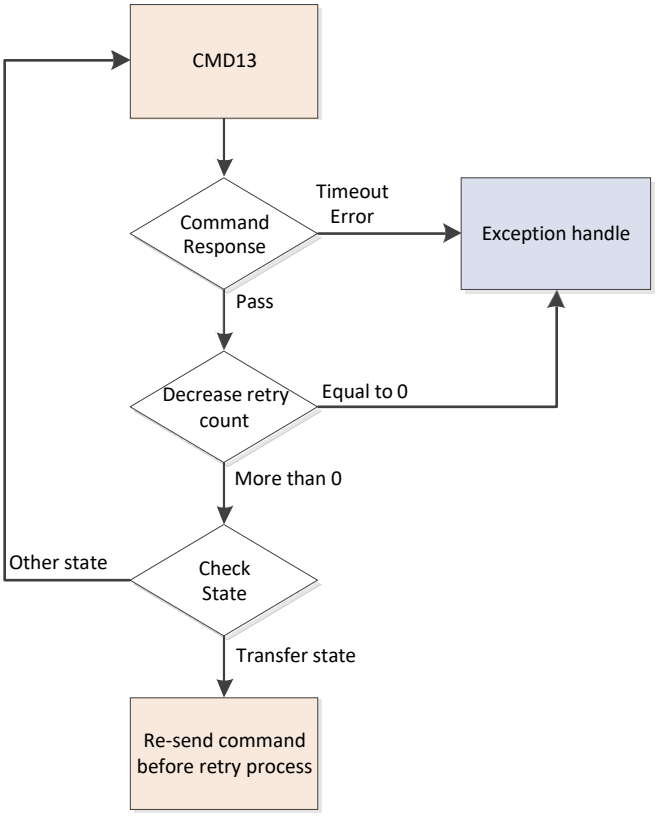


Figure 7-3 Retry Error Handling Process

7.7 Recovery Error Handling

Sometimes the device failure could not be recovered by Retry Process, it suggests to execute STOP Command (CMD12) to stop whole commands and response and then run following flow.

- Please confirm card status is in Transfer state
- In order to avoid infinite loops, host has to set up a retry counter number.

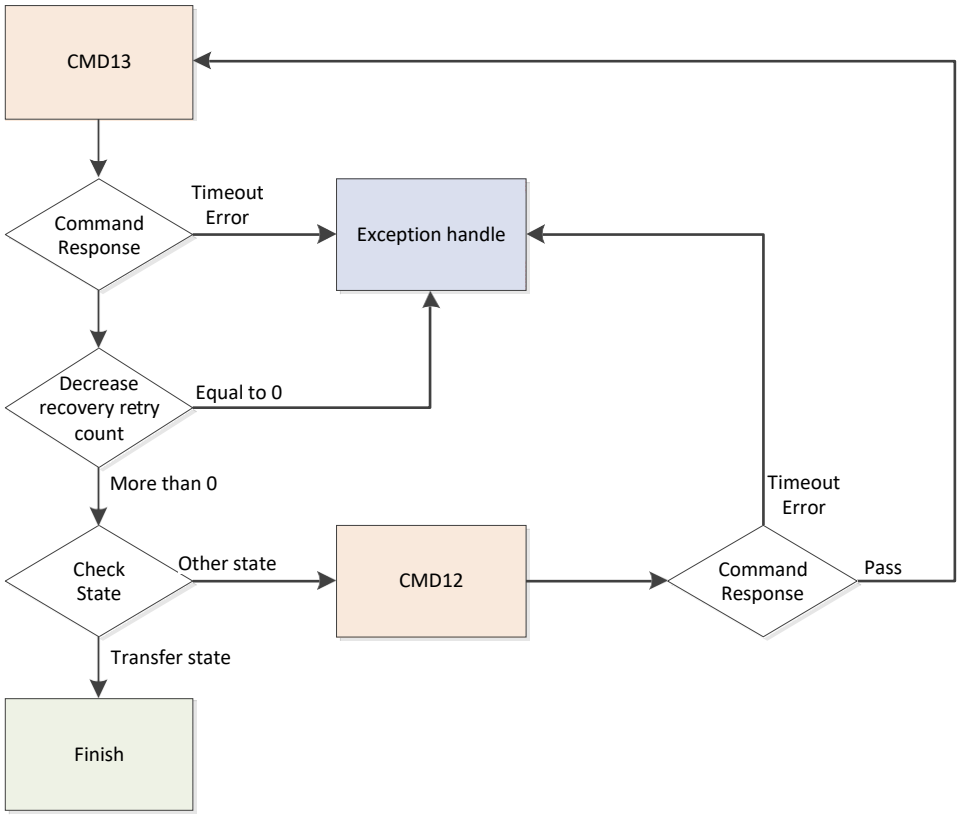


Figure 7-4 Recovery Error Handling Process

7.8 Tuning Write Command Error Handling

Reconfirm the card's pass range, to make sure card could receive host commands.

- If there was no any pass window, it might be connect issue or signal issue
- Pass Range depends on frequency level, higher frequency makes fewer pass range

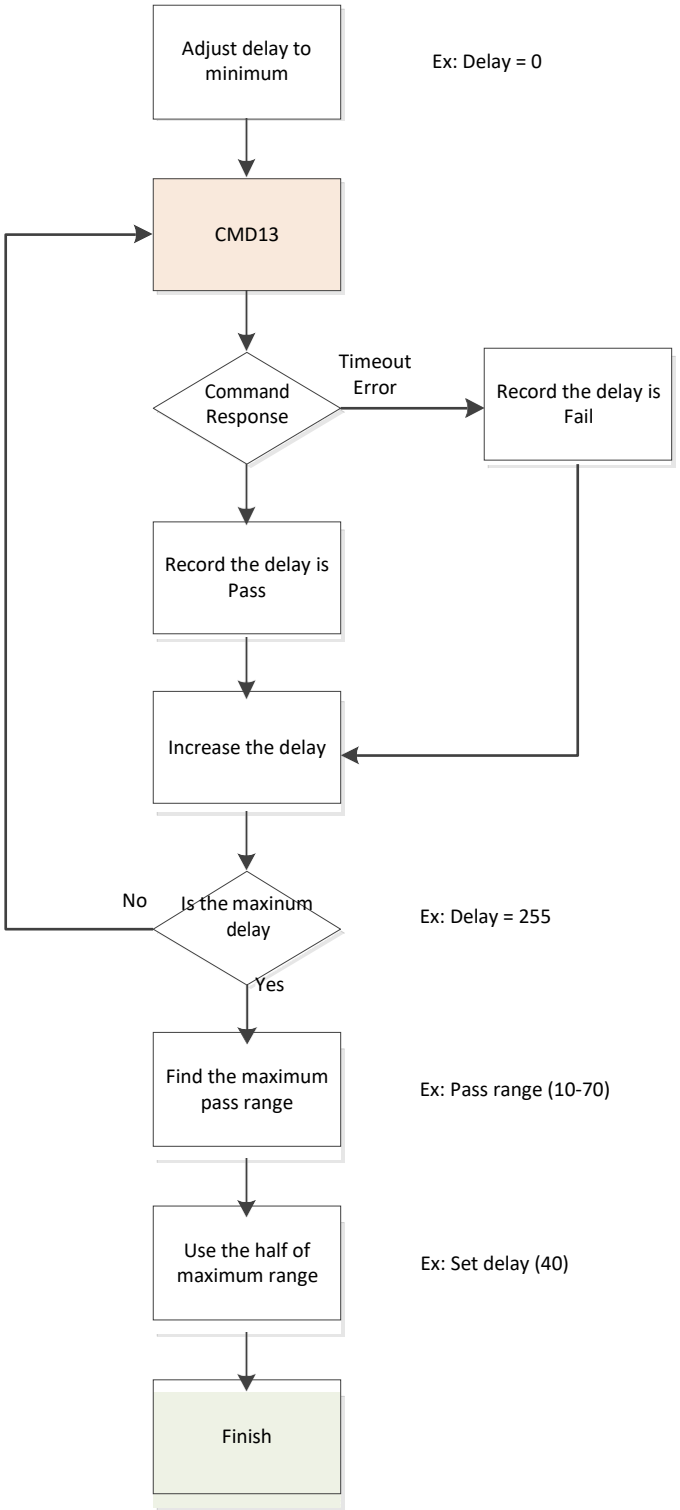


Figure 7-5 Tuning Write Command Error Handling Process

7.9 Exception Error Handling

- Error in Card's response or data output time-out, it could re-initialize the card.
- If there was CMD CRC7 issue, it could use tuning write command process to find out appropriate timing.
- If there was DAT CRC16 issue, it could use tuning read command process to find out appropriate timing.

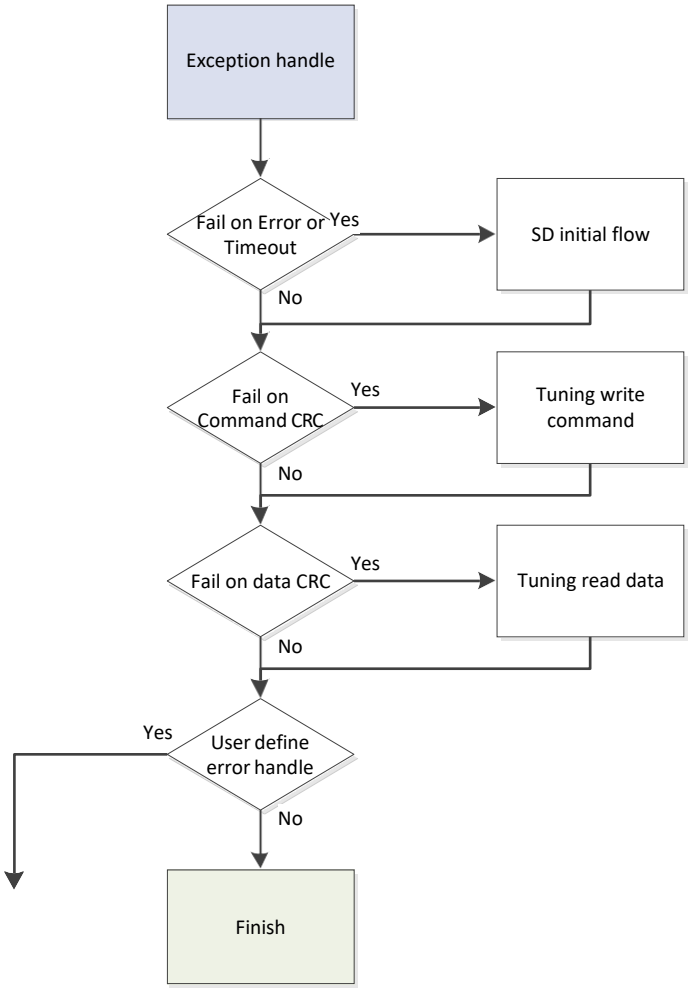


Figure 7-6 Exception Error Handling Process

7.10 Multiple Blocks Read (CMD18) Error Handling Process

- If card responded ADDRESS_OUT_OF_Range, please check reading address
- If card responded DEVICE_IS_LOCKED, please stop reading data
- If card responded COM_CRC_ERROR, run Retry or Tuning Process

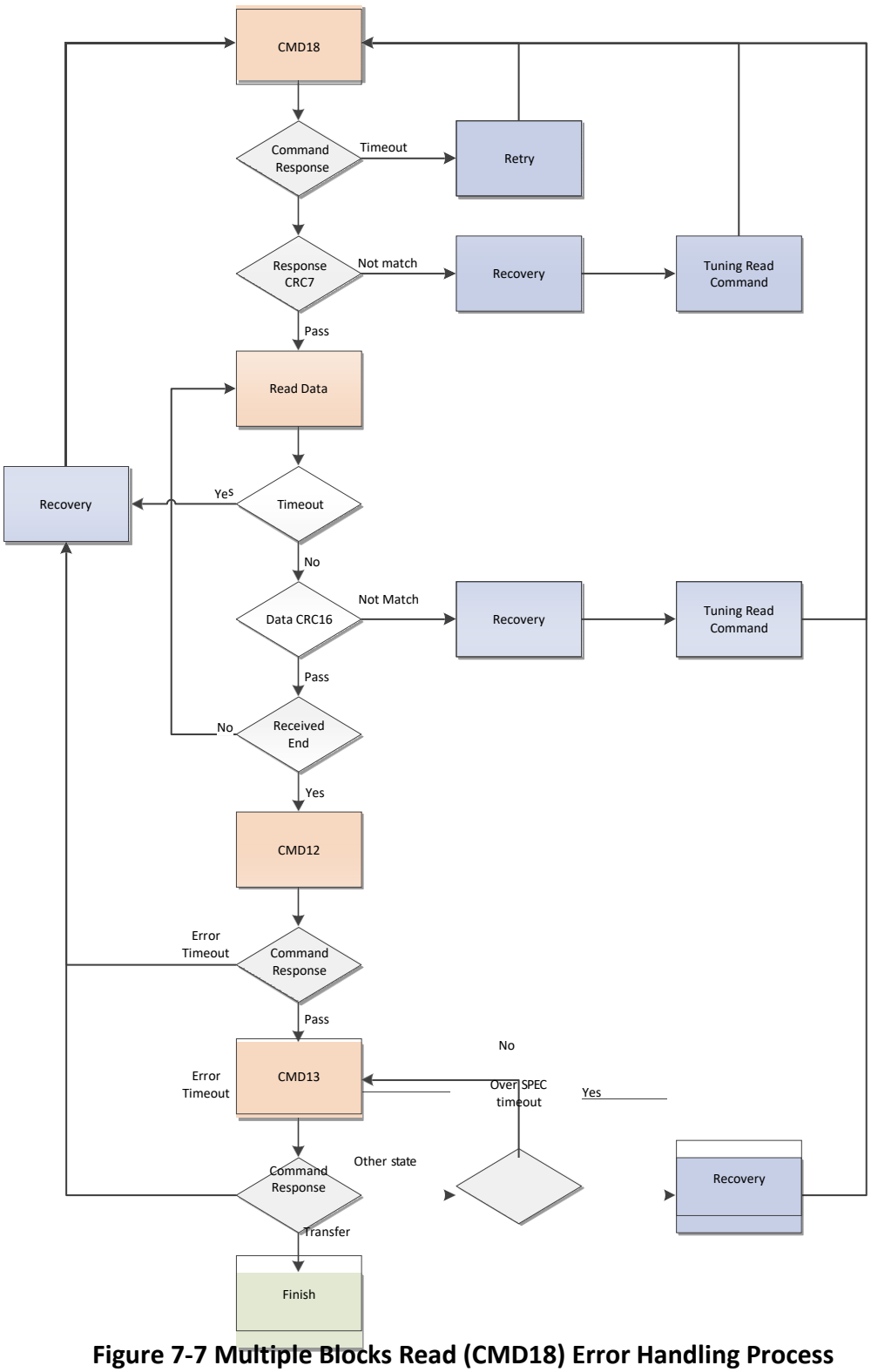


Figure 7-7 Multiple Blocks Read (CMD18) Error Handling Process

7.11 Tuning Read Data Error Handling

Reconfirm the card's pass range, to make sure host could receive card's Response and Data.

- If there was no any pass window, it might be connect issue or signal issue
- Pass Range depends on frequency level, higher frequency makes fewer pass range

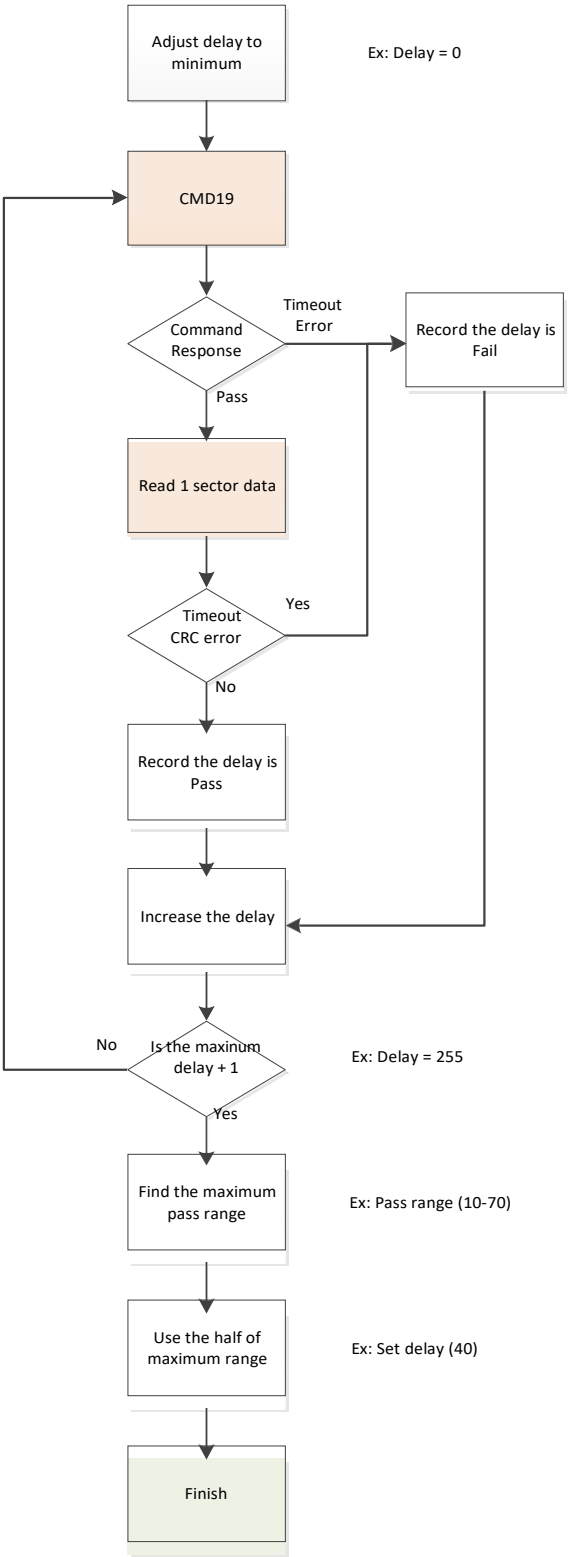


Figure 7-8 Tuning Read Data Error Handling Process

7.12 AC Coupling Capacitors Placement of Host side

AC coupling capacitors for PCIe Gen3 is defined 176nF to 265nF. According the SD spec, host side should implement the coupling capacitors of TX side of SD Express card (Rx of host side). The placement shall be as close as possible to the connector and up to 12.5mm from the connector's SD contact pads.

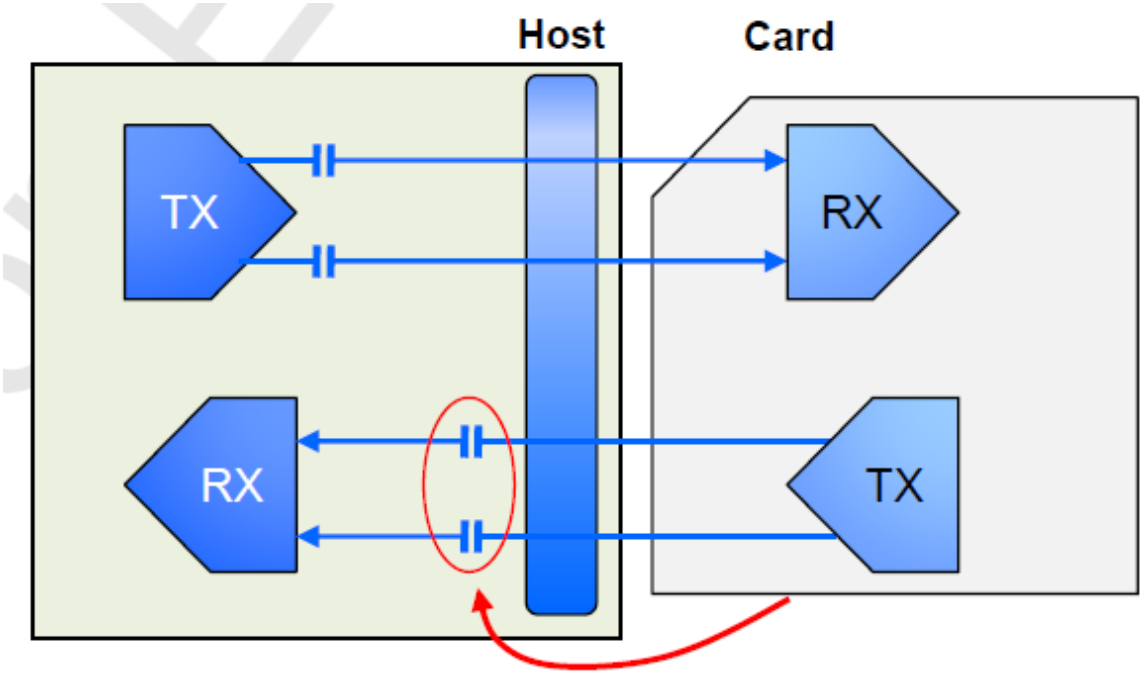


Figure 7-9 Placement of AC coupling capacitors of SD Express host

8 REGISTERS

8.1 Card Registers

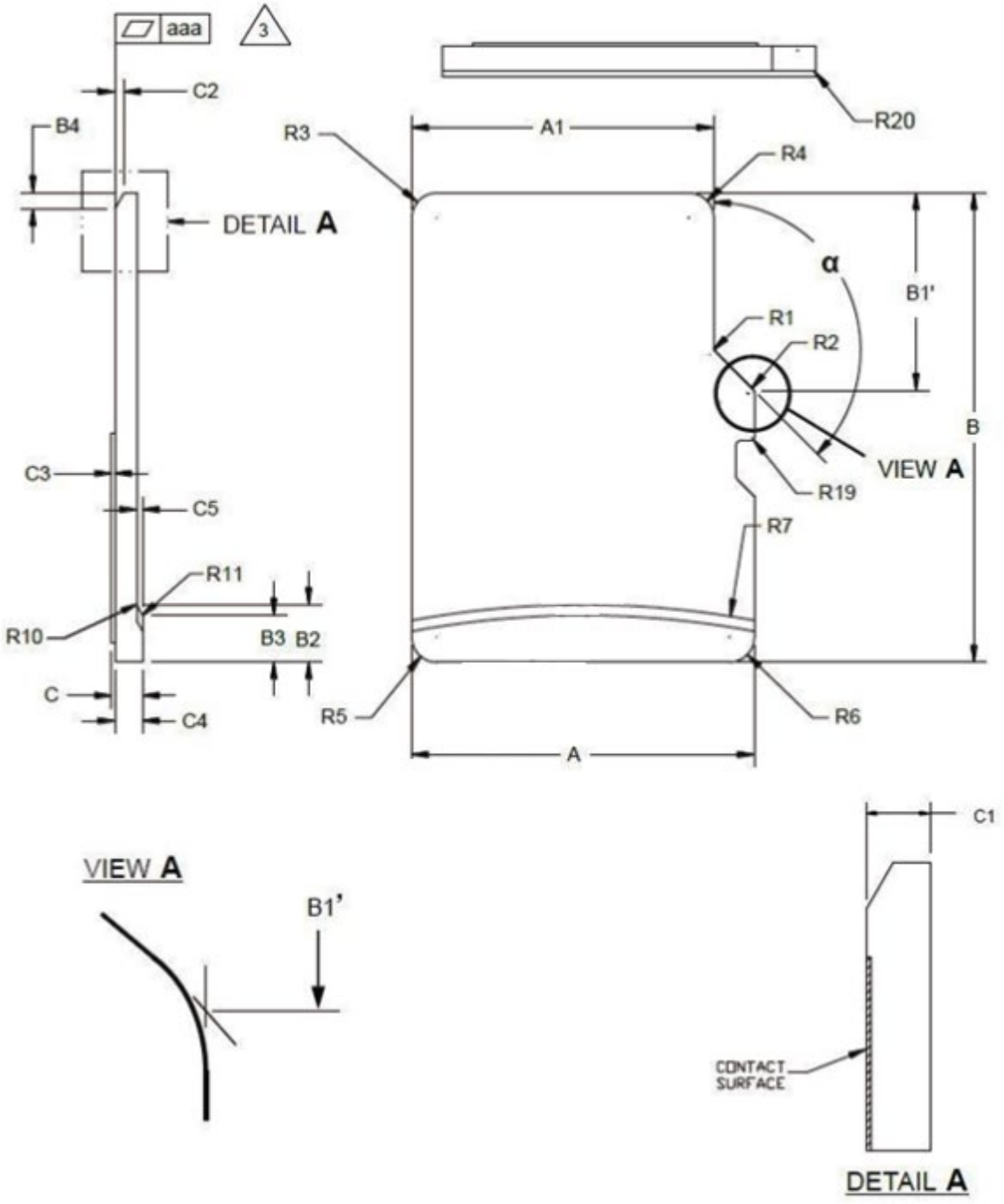
Name	Width	Description
CID	128bit	Card identification number; card individual number for identification. **Mandatory**
RCA[1]	16bit	Relative card address; local system address of a card, dynamically suggested by the card and approved by the host during initialization. **Mandatory**
DSR	16bit	Driver Stage Register; to configure the card's output drivers. **Optional**
CSD	128bit	Card Specific Data; information about the card operation conditions. **Mandatory**
SCR	64bit	SD Configuration Register; information about the SD Memory Card's Special Features capabilities **Mandatory**
OCR	32bit	Operation conditions register. **Mandatory.**
SSR	512bit	SD Status; information about the card proprietary features **Mandatory**
CSR	32bit	Card Status; information about the card status **Mandatory**

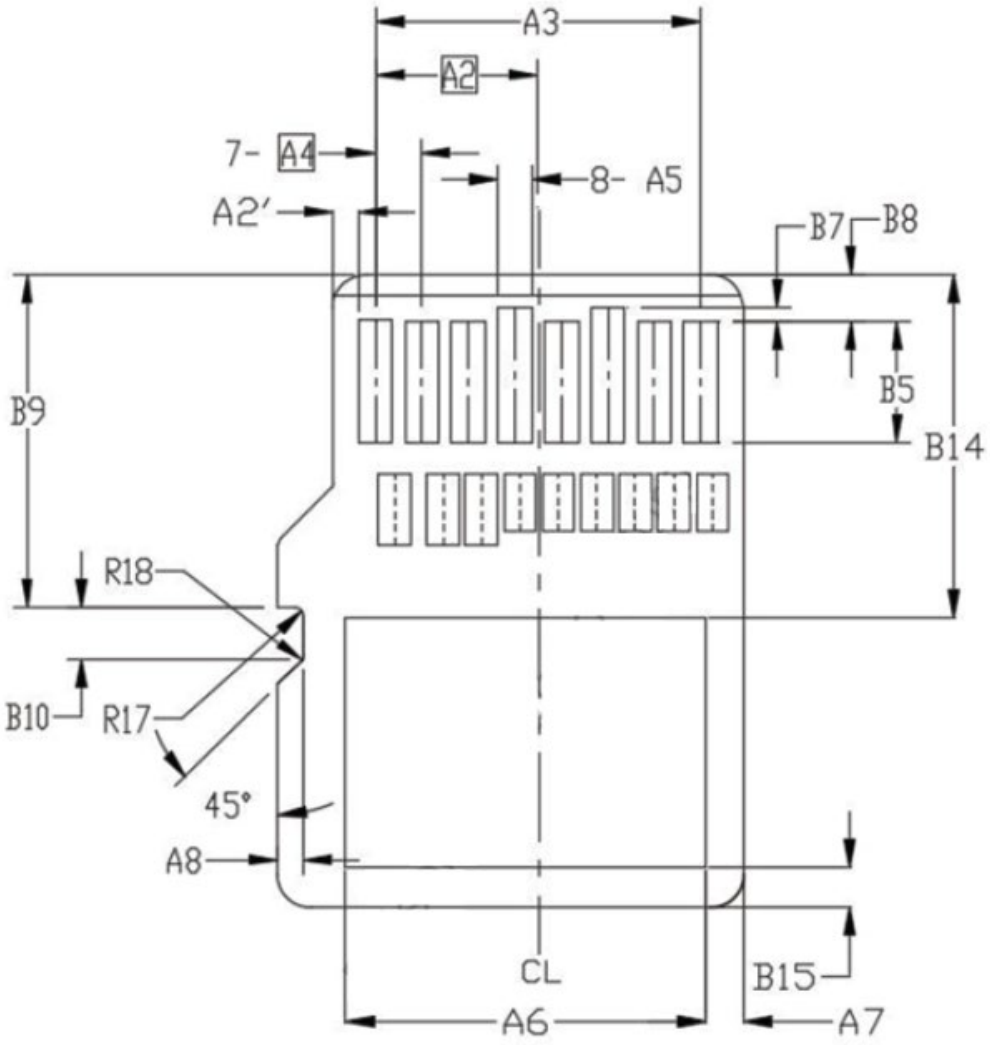
(1) RCA register is not used (or available) in SPI mode.

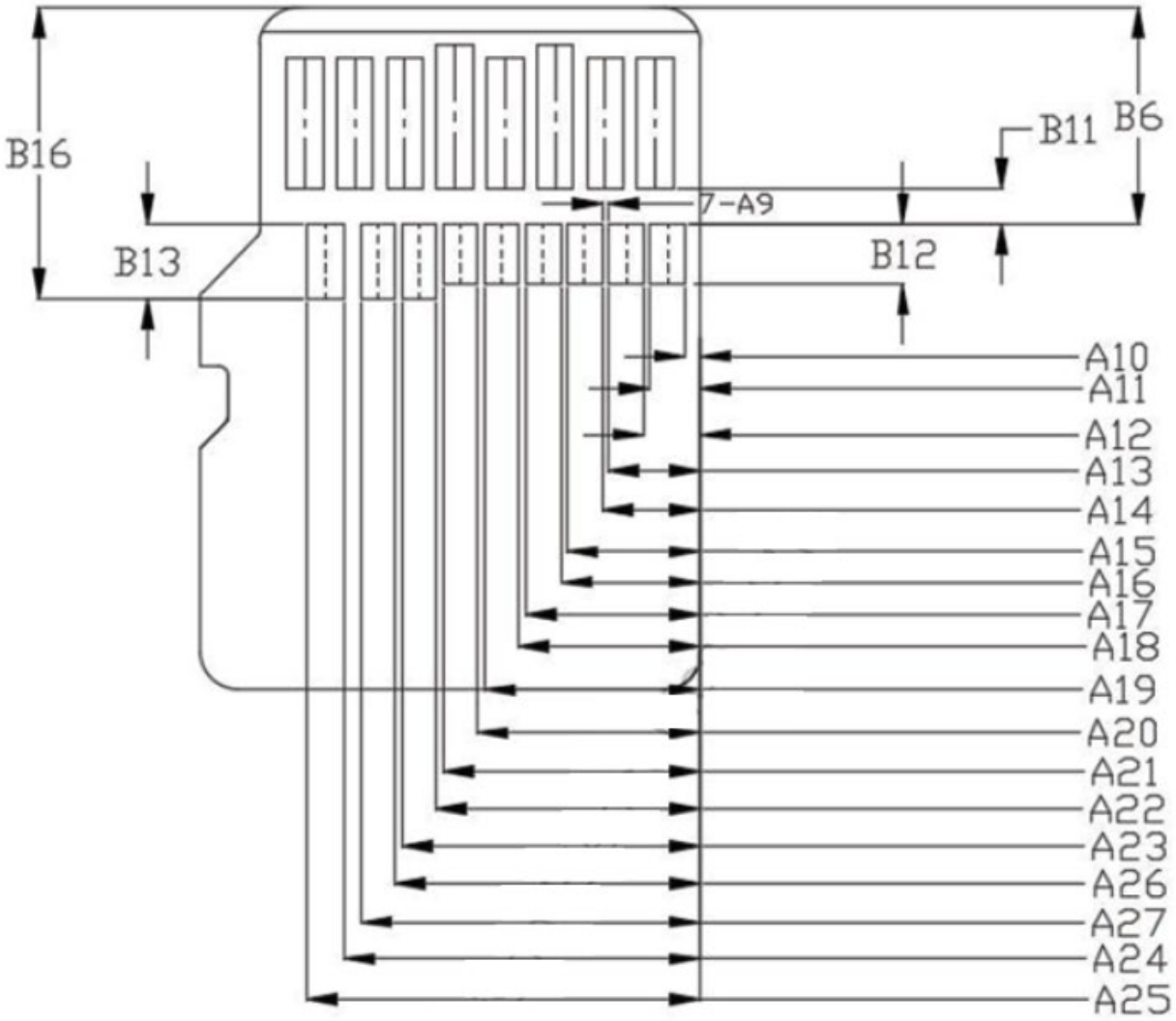
8.2 SD to NVMe Identification Registers

Register	SD	NVMe mapping (Identify Controller Data Structure)	NVMe Size	Comments
MID	MID	VID	2 bytes	VID/MID shall identify the same manufacturer
OID	OID	SSVID	2 bytes	SSVID/OID shall identify the same manufacturer
PNM	PNM	MN [0:4]	40 ASCII	MN [7:49] is vendor specific
PRV	PRV	FR [0:1]	8 bytes	FR [2:7] is vendor specific
PSN	PSN	SN [0:7]	20 ACSII	
MDT	MDT	SN [8:10]		SN [11:19] = 0
Device Size	CSD/C_SIZE	NCAP		SD/PCIE is same capacity
SD Version	SCR	NM [5:6]		MN [5] = major spec. MN [6] = minor spec.

9 PHYSICAL DIMENSION




A3
A2
7- A4
8- A5
A2'
B7
B8
B9
B5
B14
R18
B10
R17
45°
A8
CL
B15
A6
A7


B16
B11
B6
7-A9
B13
B12
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
A22
A23
A26
A27
A24
A25

	COMMON DIMENSION			
SYMBOL	MIN	NOM	MAX	NOTE
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.05	-	-	
A10	0.25	0.35	0.45	
A11	1.01	1.11	1.21	
A12	1.16	1.26	1.36	
A13	1.92	2.02	2.12	
A14	2.07	2.17	2.27	
A15	2.83	2.93	3.03	
A16	2.98	3.08	3.18	
A17	3.74	3.84	3.94	
A18	3.89	3.99	4.09	
A19	4.65	4.75	4.85	
A20	4.80	4.90	5.00	
A21	5.56	5.66	5.76	
A22	5.71	5.81	5.91	
A23	6.47	6.57	6.67	
A24	7.75	7.85	7.95	
A25	8.55	8.65	8.75	
A26	6.62	6.72	6.82	
A27	7.38	7.48	7.58	
A28	-	-	0.50	
A29	-	-	0.50	
B	14.90	15.00	15.10	
B1'	6.13	6.23	6.33	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	-	4.75	4.85	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	7.80	7.90	8.00	REF
B10	1.10	1.20	1.30	
B11	-	0.75	-	
B12	-	1.35	-	
B13	-	1.65	-	
B14	9.00	-	-	
B15	0.10			
B16	-	6.40	6.50	
B17	11.40	11.50	11.60	
B18	-	-	0.50	
C	-	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
C4	0.80	-	1.10	

Notes:

1. DIMENSIONS and TOLERANCING per ASME Y14.5M-1994.
2. Dimensions are in millimeters.
3. COPLANARITY is additive to C1 MAX thickness.
4. All edges shall not be sharp as tested per UL1439 "Test for Sharpness of Edges on Equipment"
5. As B16 is related to connector specification, this length will be defined in next version.

C5	0.15	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.60	0.80	0.90	
R6	0.60	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	
R20		-	0.15	
α	133°	135°	137°	
β	43°	45°	47°	
aaa	-	-	0.10	

10 PRODUCT WARRANTY POLICY

For any other products manufactured and supplied by KODAK (“KODAK Products”), KODAK hereby certify that in the event KODAK Product does not conform to the specification for (A) a period instructed by KODAK or mutually agreed by KODAK and the customer in writing or (B) the period ending on the date at which customer’s use of a KODAK Product exceeds KODAK Product’s total Terabytes Written as recorded by or derived from KODAK Product’s S.M.A.R.T. Attribute, including but not limited to, KODAK Product ’ s drive life is used up in accordance with the S.M.A.R.T.
Attribute, whichever occurs earlier(“Warranty Period”) and such inconformity is confirmed by KODAK to be solely attributable to KODAK, KODAK agrees to repair or replace the nonconforming KODAK Product, free of charge.